Doping-selective etching of silicon for wafer thinning in the fabrication of backside-illuminated stacked CMOS image sensors

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***Abstract*—**Backside illuminated (BSI) 3D stacked CMOS image sensors are of significant interest for various applications including light detection and ranging (LiDAR). One of the important challenges in the 3D integration of these devices involves well-controlled backside thinning of the single photon avalanche diode (SPAD) wafers, which are stacked with CMOS wafers. Backside wafer thinning is usually accomplished by a combination of backgrinding and doping-sensitive wet chemical etching of silicon. In this study, we have developed a wet etch process based on tailored $HF:HNO_3:CH_3COOH$ (HNA) chemistries, capable of achieving etch stop at a p+/p silicon transition layer with high doping-level selectivity (>90:1). Feasibility of excellent total thickness variation of ~300 nm is demonstrated across a 300 mm wafer. In addition, well-known properties of HNA-etched silicon surfaces including staining and surface roughness are characterized. Finally, a wet chemical tip-etch method for reducing surface roughness is proposed.

Keywords—backside illuminated CMOS image sensors, silicon wafer thinning, isotropic silicon etching, HNA etching

I. INTRODUCTION

Backside-illuminated (BSI) stacked CMOS image sensors are an important product category in the emerging 3D stacked image sensor market, with manifold applications. In addition to being widely used in consumer electronic devices including camera-enabled mobile phones and digital cameras due to their improved performance, power efficiency and low footprint, they also find use in automotive laser image detection and ranging (LiDAR) applications.

The 3D integration approach to the fabrication of BSI CMOS image sensors allows for the separate fabrication of single photon avalanche diode (SPAD)-based sensor wafers and CMOS readout circuitry, which are then bonded using hybrid bonding techniques. Typical process flows for fabricating 3D stacked BSI sensors have been described in detail elsewhere [1,2]. One of the important process technologies required for maximizing light coupling with the substrate and achieving high quantum efficiency is silicon wafer thinning. In this process, the SPAD wafer typically needs to be thinned down to a remaining wafer thickness on the order of the optical pixel size, usually under 10 µm. In addition, excellent cross-wafer uniformity, a damage-free surface, and good wafer-to-wafer repeatability is required to achieve a high yield process. Wafer thinning is typically done using a combination of silicon backgrinding, wet etching, and chemical mechanical planarization (CMP) to achieve the above attributes [2].

In many versions of the process, the SPAD devices are fabricated on a low-doped (p-) epitaxial silicon film deposited over a high-doped (p+) silicon bulk substrate, with the epitaxial film thickness <10 µm. The non-active side of the wafers is backgrinded to an intermediate thickness and subsequently wet chemical etched to the final thickness, with the p- epitaxial film acting as an effective etch stop layer for the chemical etch. This may be followed by steps that can result in desired surface roughness such as a CMP process.

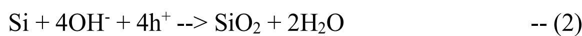
A well-known family of chemical formulations that can offer high selectivity between the p+ bulk silicon and the p- etch stop layer is $HF:HNO_3:CH_3COOH$ (HNA). In general, HNA is known to etch high-doped silicon significantly faster than low-

doped silicon, as demonstrated by other researchers [3, 4]. By suitably adjusting the $HF:HNO_3:CH_3COOH$ composition, the selectivity between p+ and p- silicon can be controlled. Combined with a sharp and well-controlled p+/p- transition doping profile, high cross-wafer uniformity can be achieved, theoretically limited only by the uniformity of the deposited epitaxial film.

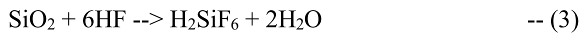
In the HNA ternary mixture, the three main compounds play different roles. The simplified silicon etching mechanism using HNA can be described as follows [5, 6, 7].

First, HNO_3 acts as an oxidant. Silicon is oxidized by the generation and injection of holes as described in equations (1) and (2). Subsequently, the oxide is dissolved by means of HF, as shown in equation (3).

$$HNO_3 + H_2O + HNO_2 \dashrightarrow 2HNO_2 + 2OH^- + 2h^+ \quad \text{-- (1)}$$



$$Si + 4OH^- + 4h^+ \dashrightarrow SiO_2 + 2H_2O \quad \text{-- (2)}$$



$$SiO_2 + 6HF \dashrightarrow H_2SiF_6 + 2H_2O \quad \text{-- (3)}$$

As can be seen, acetic acid does not actively take part in the Si etching mechanism. In the absence of acetic acid, a fresh silicon surface in HF-based solutions is expected to have hydrophobic properties. Acetic acid serves as a solvent for HF and HNO_3 and enables better wetting of silicon.

The ease with which hole generation occurs is the key criteria determining selectivity. In particular, the ratio of HF and HNO_3 as well as their overall concentration in the ternary mixture has a major influence on the p+/p- selectivity, as can be seen in the work from Bahena et al. [7]. They have demonstrated p+/p- ([B] $=10^{19}$ $cm^{-3}/10^{15}$ cm^{-3}) etch selectivity of upto 22.5 in a 1:3:8 HNA solution. Charavel and Raskin have studied the etch rate of silicon samples of various doping levels in etchants including 1:1:2 HNA. In this solution, they have reported nearly monotonic increase in silicon etch rates with boron doping concentration in the range of $5x10^{16}$ cm^{-3} to $2x10^{19}$ cm^{-3}, with an inferred selectivity of 5:1. Their work suggests that the wider the doping concentration difference between the high-doped and low-doped films, better can be the selectivity [3]. In the specific context of silicon wafer thinning by etch stop mechanism at a p+/p- interface, it has been suggested that good etch stop can be achieved when there is atleast a 10X difference and preferably a 100X difference in resistivity between the high-doped substrate and the low-doped etch stop layer [8].

In the current study, we examine the thinning of high doped (p+) silicon wafers and demonstrate the etch stop behavior of highly selective HNA-based chemical formulations at the transition between high-doped (p+) bulk silicon and low-doped (p-) epitaxial silicon films on 300 mm wafers. In addition, we discuss some typical surface characteristics of the thinned wafers, including surface staining and wafer roughness, and strategies to mitigate these issues.

II. Materials and Methods

A. Preparation of substrates

All the experiments were carried out using 300 mm silicon substrates. In the first stage of the study, bulk silicon substrates with p+ doping and epitaxial silicon films with p- doping were used for etch rate and selectivity studies with various HNA chemical compositions.

Subsequently, model bonded wafer samples were prepared as illustrated in **Fig. 1**, for wafer thinning and etch stop studies. Silicon epitaxial wafers (300 mm diameter) consisting of a known thickness of low-doped epitaxial film (p-) deposited on high-doped bulk silicon (p+) were procured from a commercial substrate vendor. For wafer handling purposes, the epitaxial surface of these target wafers was fusion bonded with a silicon carrier wafer via a TEOS interlayer, as shown in Fig. 1, using a 300 mm fusion bonder tool (TEL Synapse S, Tokyo Electron, Japan). Next, the high-doped bulk silicon in the target wafer was backgrinded down to a nominal target wafer thickness of ~ 25 um, using a Disco backgrinder tool (Disco DGP8761, Disco Corporation, Japan). These wafers were used for subsequent wafer thinning studies.

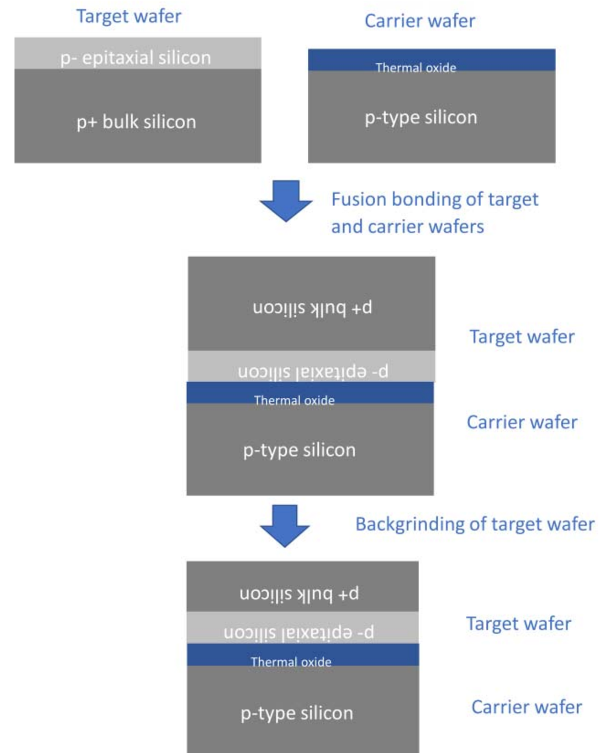


Fig. 1. Schematic illustration of the model bonded wafer preparation process.

B. Preparation of Chemistry

HF (49%), HNO_3 (69%), and CH_3COOH (glacial) were procured from commercial vendors (Tee Hai Chem Pte. Ltd., Singapore; Megachem Ltd., Singapore) and mixed externally in required volumetric proportions in 40 L batches.

C. Wet Etch Equipment Setup

All the wet etch experiments were conducted on the NexGen MG22-300 single-wafer spin-etch platform (NexGen Wafer Systems Pte. Ltd.). Owing to the autocatalytic nature of the reaction of HNA with silicon, precise process control is of the highest importance to avoid runaway reactions [9]. By using a batch process, uniform heat dissipation on adjacent wafers becomes even more challenging with increasing wafer diameter. Thus, a single wafer spin process such as the one used in this study is well-suited for this application.

The HNA chemistry was dispensed on the target wafer with a 40 to 60% dispensing profile at a flow rate of 1300 mL/min and a chuck rotation speed of 350 rpm. The wafers were etched for a fixed duration of time, determined from the etch rate of the particular chemical formulation. Subsequently, the wafers were thoroughly rinsed with DI water at a flow rate of 1300 mL/min and dried in N_2 stream. The temperature of all the experiments was maintained at 25 ^{0}C +/- 1 ^{0}C.

D. Target wafer characterization

The final silicon thickness of the target wafer was measured using a spectroscopic ellipsometer (SFX200; KLA Tencor). Surface staining of the wafer surface observed during the intermediate steps of the wafer thinning process was studied using Scanning Electron Microscopy. Further, the surface roughness of the target wafer following wafer thinning was characterized using Atomic Force Microscopy (Veeco Dimension 5000 Atomic Force Microscope, Veeco Instruments).

III. Results And Discussion

A. Etch Rate and Selectivity Studies on Blanket Wafers

Based on the HF:HNO_3:CH_3COOH mixing triangle of Robbins and Schwartz [6], four different HNA compositions were prepared and the p+/p- selectivity was determined.

The HNA starting composition 1 consisted of 10% HF, 41% HNO_3 and 49% acetic acid. For compositions 2 to 4, the HF percentage was kept constant, the proportion of HNO_3 was gradually increased, while the ratio of acetic acid correspondingly reduced (Fig. 2).

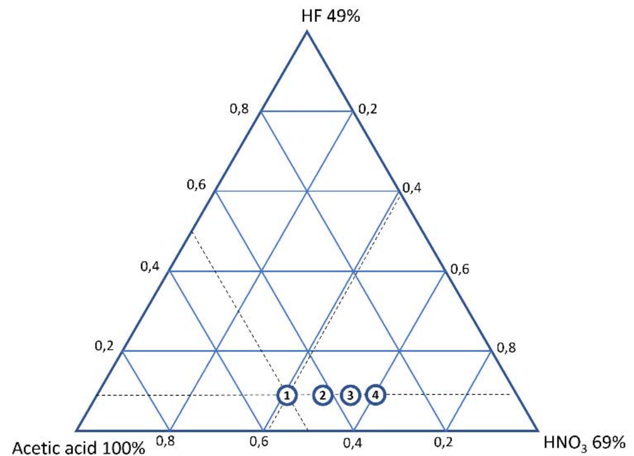


Fig. 2: HNA mixing triangle representing various compositions studied in this work.

The selectivity of each HNA composition was determined as the ratio of the etch rates of silicon blanket wafers with p+ and p- doping. The wafers were etched for a fixed duration of 3 min for these studies.

The selectivity results are shown in Table 1. As can be seen from the table, the starting composition neither etched the p+ nor the p- blanket wafers.

Table 1. Etch rate and selectivity of various HNA compositions at 25 ^{0}C.

Composition	Average p+ etch rate (µm/min)	Average p- etch rate (µm/min)	Average selectivity
1	0	0	NA
2	3.8	0.04	95:1
3	4.6	0.05	90:1
4	6.2	0.1	62:1

By keeping the HF concentration constant and increasing the HNO_3 concentration, the p+ and p- silicon finally started to etch (composition 2). Further increase in the HNO_3 ratio caused even faster etching of both p+ and p- silicon, resulting in a drop in p+/p- selectivity from 95:1 for composition 2 to 62:1 for composition 4.

Those results are consistent with the findings of Bahena et al. [7], showing that an increase in etch rate of p+ silicon is often accompanied by a loss of selectivity to p- silicon. Based on these initial results, we chose to use composition 2 for all the subsequent experiments.

B. *Etch Stop on Bonded Wafers*

The etch stop behavior of composition 2 on bonded and backgrinded wafers, prepared according to the procedure shown in Fig. 1, was studied next. To better understand the transition at the p+/p- interface, the wafer to be thinning (henceforth referred to as target wafer) was progressively etched in composition 2 with intermediate thickness measurements. The results are shown in Fig. 3. While nearly linear etch at high etch rate (~3.8 µm/min) was seen as the high-doped bulk silicon was removed, at a certain point, an abrupt drop in etch rate to <40 nm/min was observed, suggesting that the etch stop layer at the p+/p- had been reached. This result demonstrated the feasibility of good etch stop at the p+/p- transition region.

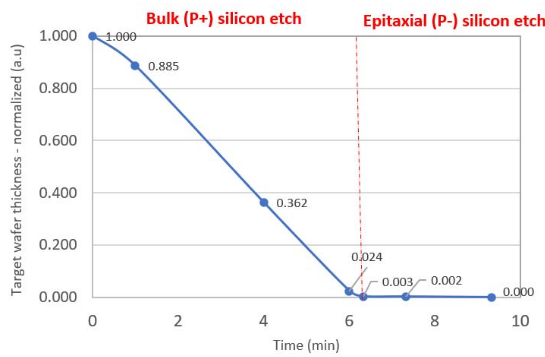
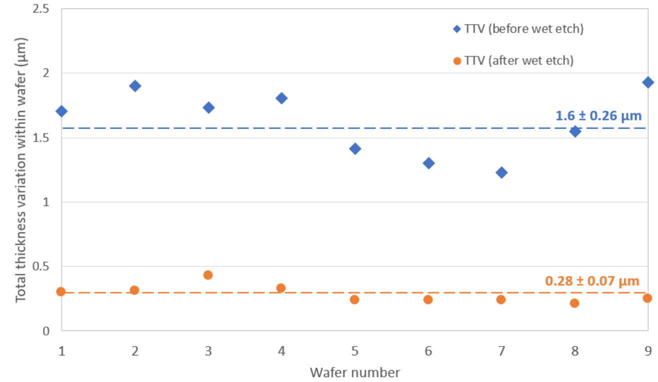
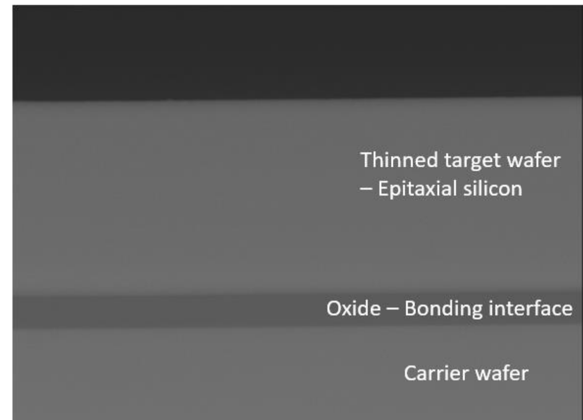


Fig. 3: Evolution of target wafer thickness (normalized and expressed in arbitrary units) etched in composition 2, showing linear etch in bulk silicon and etch stop at the epitaxial film interface.

Subsequent wafers were etched for a fixed time duration, calculated based on the etch rate and incoming target wafer thickness. Fig. 4(a) shows the total thickness variation (TTV) within wafer measured for 9 samples, incoming to wet etch (i.e., after backgrinding) and after the wet silicon etch process. The within-wafer TTV was calculated by measuring the target wafer thickness at 49 sampling locations across the wafer and calculating the statistical range of the measurements. The incoming average TTV across the 9 wafers was observed to be ~1.6 µm, with a wafer-to-wafer standard deviation of 0.26 µm). On the other hand, the average TTV across the same wafers after wet etch was calculated as 0.28 µm, with a wafer-to-wafer standard deviation of 0.07 µm, exhibiting significant improvement over the incoming TTV values. These results demonstrate the feasibility of achieving excellent TTV of <300 nm with the etch-stop strategy. It is worth noting that the TTV obtained post wet etch is similar to typical cross-wafer uniformities measured for epitaxial silicon films across 300 mm wafers. A cross-sectional SEM image of the final thinned wafer is shown in Fig. 4(b).



(a)



(b)

Fig. 4: (a) Total thickness variation within wafer before wet silicon etch (after backgrinding) and after wet silicon etch (TTV is calculated based on 49 sampling locations within wafer per measurement), **(c)** Cross-sectional SEM image showing the thinned target wafer.

C. *Wafer Staining*

As the high-doped silicon was etched in HNA solutions, a brown staining film was observed on the wafer surface (**Fig. 5(a)**), an observation consistent with reports by other researchers. A top-down SEM image of the brown stain region shown in **Fig. 5(c)**, appears to indicate a rough, potentially porous surface, which can be detrimental for our target application. This morphology is also consistent with reports by other researchers, and it has been speculated that this film is composed of non-stoichiometric high surface area silicon oxides, spanning ~10-20 nm thickness at the wafer surface. It has been shown that the stain film can be removed in alkaline solutions such as NH_4OH, albeit with some additional silicon loss [7].

However, for our present application, good thickness control of the target wafer is essential and additional silicon loss may need to be minimized as far as possible, once the etch stop doping concentration is reached. In our experiments, we observed that once the etch stop layer was reached, the staining can be significantly reduced simply by adding overetch in the HNA solution, as shown in **Fig. 5(b)**. This is attractive owing to process simplicity and can be achieved with minimal silicon loss as the etch rate of silicon at the etch stop layer is very low.

The results indicate that the formation of this porous stain film is strongly influenced by the substrate resistivity. We hypothesize that as more of the high resistivity substrate is exposed on the wafer, the rate of formation of the porous film slows down significantly until the rate of removal of the porous film in the HNA solution exceeds the rate of formation of the new film. This ultimately results in the removal of the stain film.

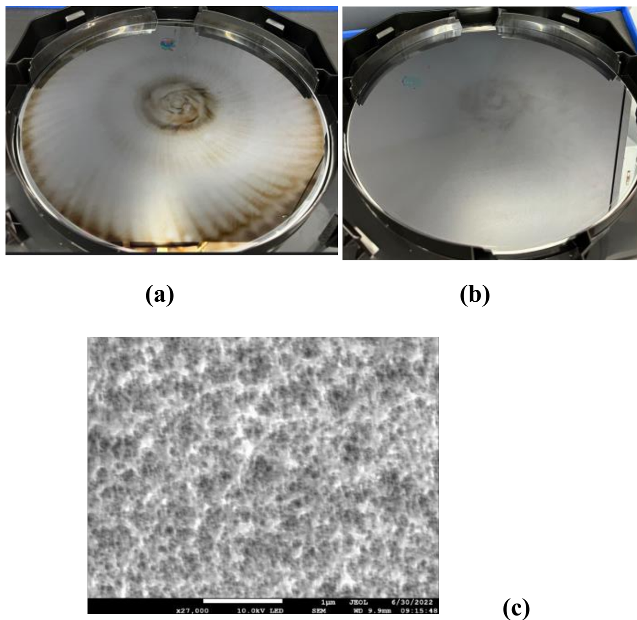


Fig. 5: Optical images showing (a) brown staining on the etched wafer surface during the process, (b) brown staining mitigated with overetching on the same wafer, (c) SEM image of the wafer staining

D. Wafer Roughness Post-etching

Post-etching roughness of the p- stop layer was measured with AFM on silicon coupons obtained from the bonded wafers. In total, 7 silicon coupons were measured under various experimental conditions (**Fig. 6**).

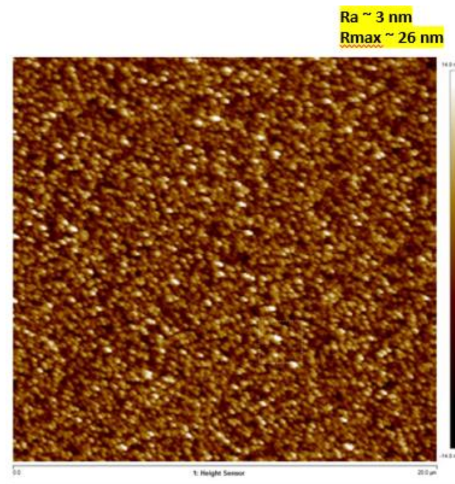


Fig. 6: AFM measurement of surface roughness post wet etching, with average Ra ~3 nm and R_{max} ~ 26 nm, measured across 2 µm x 2 µm sampling area.

Over all the samples studied, the average roughness (R_a) was measured as ~3.19 nm, ranging from 2.06 nm up to 4.34 nm, whereas the average maximum roughness (R_{max}) was ~26.23 nm, ranging from 16.90 nm up to 38.20 nm. The area used for measuring the roughness parameters was 2 µm x 2 µm.

While this is comparable with reports in the literature and in general, HNA-etched surfaces are often described as mirror-like surfaces, optical devices require much tighter roughness specifications [11]. Further attempts to improve the roughness with the HNA process is not recommended as changes in the HNA composition are likely to alter the etch stop process in terms of selectivity and etch rate.

In typical process integration schemes for 3D stacked BSI CMOS image sensors, surface roughness is often improved by implementing an additional CMP buff step [1]. The implementation of this additional step also adds to process costs.

As a potential alternative to CMP, we have conducted some preliminary studies on a more cost-effective wet-chemistry approach to smoothen the p- stop layer without additional silicon loss. By implementing a tip-etch process, the roughness in the transition area can be improved without appreciable etching into the p- silicon [10]. The tip-etch process consists of a series of partial oxidation and oxide dissolution steps that can be performed immediately after stopping with HNA on the p- layer (**Fig. 7**).

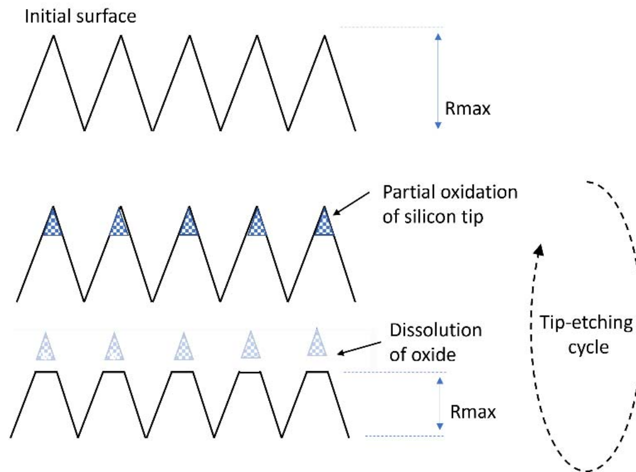


Fig. 7: Schematic illustration of the tip-etching process principle, by partial oxidation of silicon and subsequent dissolution.

By performing multiple cycles of partial-oxidation and oxide dissolution, the overall roughness can be gradually reduced.

In a series of experiments performed with test coupons obtained from bonded wafers etched to the p- transition layer, a noticeable reduction of R_{max} was observed by performing multiple cycles of tip-etching. Specifically, the tip-etching tests were performed by sequentially immersing silicon coupons in a beaker with 10 wt.% HNO_3 for a fixed duration to form oxide at silicon tip, rinsing with DI water, dissolving the freshly formed oxide layer in 25 wt.% HF and finally, rinsing with DI water again (**Fig. 8**). The coupons were subjected to this procedure 1 or 2 times with varying HNO_3 oxidation times.

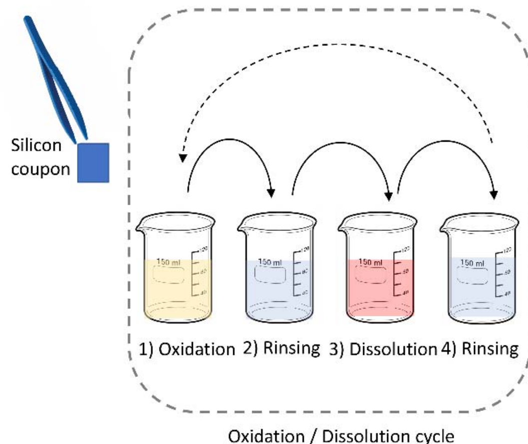


Fig. 8: Experimental setup of the tip-etching process

The roughness of the silicon coupons was measured with AFM before and after etching. The maximum roughness (R_{max}) of each coupon, measured in a 2x2 µm area, and the corresponding oxidation times are shown in **Table 2**. In most of the cases, there is appreciable decrease in R_{max} of the coupons after the above treatment. The general trends of the results indicate promise that this could be a potential method for reducing R_{max}. Further research on this topic as well as extension of this approach to full wafer testing is ongoing.

Table 2: Maximum roughness (R_{max}) before and after tip-etching

Sample #	Pre-etch R_{max} (nm)	1st HNO_3 etch (s)	2nd HNO_3 etch (s)	Post-etch R_{max} (nm)	Change in R_{max} (nm)
1	23.8	4	4	18.6	5.2
2	25.9	4	0	21.7	4.2
3	33.3	8	8	25.4	7.9
4	38.2	8	0	23.8	14.4
5	27.0	4	2	30.7	-3.7
6	35.6	4	8	17.0	18.6
7	28.4	8	4	14.1	14.3

Nevertheless, this wet chemical approach can be very attractive as it can be directly combined with the doping-selective etch, reducing total throughput time. Further, elimination of the additional CMP step may be ultimately possible, with improvements in this method.

IV. CONCLUSIONS

In this work, we have demonstrated a HNA-based wet etch process for thinning silicon wafers, with highly selective etch stop capability relying on the silicon doping difference at the transition interface. The feasibility of achieving excellent TTV of ~300 nm across 300 mm wafers has been demonstrated. Further, progress has been made in understanding and mitigating wafer staining in HNA etches. Our results show that using simple HNA overetch at the p+/p- interface can help reduce stain film formation. Finally, surface roughness post HNA etch has been studied and a wet chemical tip-etch approach is proposed as a potentially cost-effective method for reducing surface roughness. Results from coupon-level experiments shared in this paper show significant promise in reducing surface roughness and further experiments are ongoing. We believe that the results shared in this paper make important additions to the body of literature available on the silicon wafer thinning process for the fabrication of 3D stacked BSI CMOS image sensors.

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