**Kevin Nugent - BEng (Hons) First Class / MSc**

**Senior Hardware Development Engineer**

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**Core Skills**

* VHDL RTL (digital) design/integration (@Block + Chip level) - 20 years
* Creation of highly detailed design implementation documents for various projects - 18 years
* SoC/ASIC IP VHDL Development (incl. integration, front-end synthesis, static timing analysis) - 8 years
* Front-End Verification (Simulation including recently UVVM) / Formal verification (LEC) - 15 years / 8 years
* Xilinx Vivado FPGA Kintex7 / KU/VU & Zynq7 VHDL development (incl. Impl. P&R + timing closure) - 3 years
* Intel Quartus FPGA Stratix IV/Cyclone IV E,GX,V/Arria 10, CPLD MAX V VHDL development (incl. impl. P&R + timing closure) - 6.5 years
* FPGA Bench Validation using Xilinx ChipScope / Altera SignalTap II logic Analyzer - 2 years / 6 years
* Scripting languages (TCL) / Database configuration management (revision control) - 5 years / 6 years

**Other skills**

* UVVM – Generation of VHDL Bus Functional Models (BFMs) / VHDL Verification Components (VVCs)
* DSP System + Signal Processing Toolboxes in MATLAB designing FIR & IIR filters based on Filter specification requirements
* MATLAB / SIMULINK experience (completed also Onramp online MathWork courses)
* Code Coverage verification / CDC concepts / IP quality checks (including RTL coding style / CDC)
* DFT methodologies / Low power techniques / Physical Synthesis optimization techniques
* AXI4 interfaces knowledge
* Verilog knowledge
* Python knowledge
* Xilinx Vivado HLS + Vitis HLS
* Xilinx SDK + Vitis for programming the FPGA
* Microsoft Visio / PowerPoint
* Working in an agile scrum team environment
* Bilingual (fluent in English and Greek)

**Tools**

* Xilinx Vivado (IP integrator/ IP packager, Synthesis, Implementation (P&R) incl. ChipScope) - 3 years
* Quartus II Altera/Intel (including TimeQuest Timing Analyser, SignalTap II, Logic Pro Analyser) – 6.5 years
* Synopsys DC/Cadence RC/Cadence LEC Conformal/Cadence LP Conformal - 2 years/5 years/8 years/6 months
* Xilinx Vivado HLS / Xilinx Vitis HLS
* Profishark / Wireshark
* MathWorks MATLAB / SIMULINK (R2019b + R2020a/b Home edition) - (including DSP toolboxes) - 1 year
* Mentor Graphics ModelSim / Cadence NCSim / Xilinx Vivado simulators – 7.5 years / 4 years / 2 years
* SpyGlass Atrenta (for CDC) - 1 year
* Aldec Active-HDL (AHDL) / Aldec ALINT-PRO Design rule checks (DRC) - 4 months / 1 month
* SVN (Revision control tool), GIT (bitbucket) – 5.5 years / 2.5 years

**Personal Profile**

* A conscientious and ambitious professional
* A highly skilled electronics hardware engineer with 21 years of experience in hardware development activities from initial design concept to implementation
* Strongly motivated, committed, proactive, organized and enthusiastic with flexible and creative personality
* Proactive learner. Enjoy learning using new tools enhancing my career in other areas too
* Excellent skills in communication (able to communicate clearly on technical matters, written & verbal)
* Proven problem solving with very good attention to detail
* Competent time management skills
* Enjoy working as part of a multi-disciplinary team as well as the personal challenge of working independently using own initiative

**Employment History**

ASML, Wilton, CT, US. 04/11/23-Present. **Senior FPGA Engineer**

* Key individual contributor on Extreme Ultraviolet Lithography (EUV) technology machine EXE:5000 Reticle Stage project supporting FPGA development (design and verification efforts) for the High Speed Signal Processing
* Responsible for FPGA design, verification and documentation (RTL design including, Simulation/validation to verify the design + documenting/reviewing all design decisions and test results with the project team)
* Ensuring the reliability of the HSSP board / FPGA firmware (FW) through rigorous testing
* Carry on following ASML methodologies using the appropriate standards, processes, procedures and tools throughout the FPGA development life cycle
* Using GIT bitbucket (Database Configuration Management - Revision control tool) for version control of the FPGA VHDL code + other input source files/scripts incl. other FPGA DDM2 activities (Building/Archiving of FW releases)
* Comfortable with daily stand-ups where progress is reported & new actions taken

ASML, Veldhoven, Netherlands. 11/15/21-04/10/23. **Senior System Integration & Test Engineer**

* Worked closely in a cross-site development environment with ASML teams in Veldhoven and the USA
* Key individual contributor on Extreme Ultraviolet Lithography (EUV) technology machine EXE:5000 Reticle Stage project supporting FPGA development (design and verification efforts) for the High Speed Signal Processing
* Responsible for FPGA design, verification and documentation (RTL design including, Simulation/validation to verify the design + documenting/reviewing all design decisions and test results with the project team)
* Ensuring the reliability of the HSSP board / FPGA firmware through rigorous testing
* Responsible for setting up a bench testing environment in a lab and validating the Time Sensitive Ethernet Links (TSELs) HSSP firmware locating issues along its way and collaborating with key team members to resolve them
* Provided leadership to other team members by coaching them how to use specific tools (Quartus FPGA Programmer/USB blaster, SignalTap) & how to run specific bench test equipment (MINT U2T, MINT U2S) via python software scripts
* Followed ASML methodologies (ASML values, FPGA way of working etc) using the appropriate standards, processes, procedures and tools throughout the FPGA development life cycle
* Used bitbucket (Database Configuration Management - Revision control tool) for version control of the FPGA VHDL code + other input source files / scripts
* Comfortable with daily stand-ups where progress is reported & new actions taken

Siemens Healthineers, Oxford. 02/21-07/21. **Consultant FPGA Design Engineer (working from home)**

* Responsible for improvements to the existing Real Time Coil Monitor (RTCM) FPGA hardware platform used in the healthcare MRI scanner sector
* Combined CPLD ‘Flash Programming’ + ‘FPGA Configuration’ operating modes together for the existing Parallel Flash Loader (PFL) IP via the IP catalog of the Quartus II Intel tool & validated its combined functionality.
* Improved the FPGA synthesis flow by generating new Synopsys Design Constraints (SDC) and performed Static Timing Analysis (STA) checks on all required corner cases using the Quartus TimeQuest Timing Analyzer tool. Resolved all timing violations and unconstrained paths.
* Introduced a new UVVM verification platform, building from scratch a new custom VHDL Verification Environment for the FPGA. Created Bus Functional Model (BFM) procedural code & VHDL Verification Components (VVCs) in a structured way for Design Under Test (DUT) modules
* Worked in an agile scrum team of mainly 3-5 engineers & used SVN as the version control tool

Home Study. 10/19 – 01/21.

* Completion of Onramp online MathWork MATLAB/SIMULINK + Python Data Science online Udemy courses
* Design of FIR & IIR filters based on Filter specification requirements using MATLAB DSP System & Signal Processing Toolboxes
* Design of a LPF FIR for floating-point (Single & Double precision) & then Fixed-point using MATLAB Fixed-Point Designer toolbox meeting its specification requirements
* Created a blog website: <https://kevnugent.com>/about/ describing MATLAB / DSP hardware development best practices (blog website is still under development)
* Xilinx High Level Synthesis (HLS) c++ -> RTL including C synthesis + Optimization techniques to improve the throughput

EMMotorsport, Bicester. 03/19-09/19. **Senior FPGA Systems Development Engineer**

* Development of VHDL code using Xilinx Vivado tool for a new Telemetry system wrt. specification requirements
* Successful generation of user IPs from VHDL & integration of all IPs (including customized ones e.g. Reed Solomon Encoder/Decoder, Convolutional Encoder, Viterbi Decoder) in a top-level block design schematic
* Successful verification of the current system at top-level using the Vivado simulator incl. synthesis/timing closure
* Improved one of the customized IPs (Viterbi) data throughput by a factor of 12 by changing the architecture from serial to parallel. Observed this improvement in simulation

Link Microtek, Hedge End. 05/18-07/18. **Electronics Design Engineer**

* Assembly/production testing, repair work of their current products

FirstEDA Ltd, Bracknell. 09/17-02/18. **Applications Specialist**

* Customer technical support on mainly Active-HDL tool + other technical support on ALINT-PRO tool setting up few rule policy checks including STARC, DO254 reporting many RTL coding style design rule check issues for attention
* Written articles + created short demos on Code Coverage using Active-HDL tool to promote the company needs

Snell Advanced Media, Havant. 07/15-09/17. **Senior FPGA Design Engineer**

* Successful development of new FPGA VHDL features + upgrades using Xilinx Vivado tool on various broadcast ‘Video over IP’ projects. Resolved few clock domain crossing issues and achieved timing closure
* Porting the existing Xilinx Vivado platform from Kintex7 to Virtex & Kintex Ultrascale platforms as baselines
* The new ARCNET packet handler handshaking protocol implementation re-design improved the byte packet transfer rate by a factor of 9. My work is still implemented within their products today

Cadac Holdings Ltd, Luton. 06/12-03/15. **Senior FPGA Design Engineer**

* VHDL/implementation upgrades to the existing digital live audio mixing console platform for theatre use
* Mixer FPGA flow ownership using Quartus II Altera tool - Successful development of new FPGA VHDL design features, upgrades/re-designs using FIFOs + integration/impl. activities on the digital live audio mixing console

Frobas GmbH, Germany. 10/11-12/11. **Senior Design Engineer Consultant**

* Generation of Cadence CDC basic check flow scripts on an Automotive project
* Performed SoC CDC rule structural checks - Diagnosed & reported CDC rule check failures for attention

Sepura PLC, Cambridge**.** 04/10-06/11. **ASIC/FPGA Design Engineer Consultant**

* IP development (Synthesis / Formal verification) using CADENCE tools (preparations for ASIC) on a Tetra Digital Radio project**.** Successful delivery of all IP netlists (timing clean) + scripts in a version control system
* FPGA flow ownership. FPGA development (including synthesis & timing closure) using Altera Quartus II tool

NXP Semiconductors (formerly PHILIPS). 2005-2010. **Principal Digital IP Development Engineer**

* Numerous SoC IP block ownership successful development activities (VHDL design, Verilog integration, Synthesis, DFT, Formal verification (LEC) & Simulation) on multiple Set-Top-Box and HD DTV projects (using mainly CADENCE tools)
* Performed IP quality checks (RTL coding style checks, Synthesis qualification, Formal verification / CDC checks)
* Performed power domain analysis checks on a back-end netlist using Common Power Format (CPF)
* Supported other NXP sites on their IP synthesis / formal verification issues (whenever required)
* Received multiple individual/team recognition awards for my outstanding achievements to the various projects

PHILIPS Semiconductors. 1999-2005. **Senior/Principal Digital IC Development Engineer**

* Successful IC block development (VHDL Design, Synthesis & Simulation) on multiple CD/DVD projects
* Was promoted from Senior to Principal level (year 2001) wrt my successfully yearly performance reviews

PHILIPS Semiconductors. 1997-1999. **Senior Application Development Engineer**

* Successfully designed for a 1chip CDROM system new evaluation/demo boards incl. system evaluation tests

University of Hertfordshire, Hatfield. 1996-1997. **Teaching Company Associate Engineer**

* Product development (VHDL design / simulation) for a Stepper motor control system (targeting an FPGA)

American International school, Nicosia. 1994-1996. **Substitute Maths teacher.**

* Had the opportunity to teach Maths at all school levels whilst I was seeking employment in my own field

Mitel Telecom Ltd. Newport. 1993. **Research Engineer in Microelectronics**

* Introduction of Flip-Chip technology and fine line screen printing on a ceramic substrate / wafer
* Planned for the provisioning of new equipment / materials and arranged for delivery and installation
* New product development - MSc thesis industrial placement. Successful completion of MSc thesis

Monsanto PLC, Newport. 1991. **Electrical/Instrument Design Engineer**

* Involved in the original design, CAD design, procurement of equipment, installation and commissioning

**Education**

* MSc in Electronic Production Engineering (Awarded full scholarship by the University)
* BEng (Hons) Electrical & Electronic Engineering, 1st Class (Awarded scholarship by the Cyprus government)
* Diploma of Technician Engineer in Electrical Engineering (HND equivalent)
* Leaving Certificate Secondary Education, Average grade 86% (Maths, Physics, Chemistry, English)
* GCE A’ Level Pure Maths, Grade A

**Interests**

Acrylic art landscape painting, Jive dancing, DIY, keep fit (gym, rowing / circuit training, cycling, long walking & jogging), meeting people from a wide range of cultures, travelling (Europe, Australasia, USA), cycle-to-work

**References available upon request**