INTUITIVE deliverable report D4.7

Ultra-thin chips-based sensory interface

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Summary

The ESR's contribution to the INTUITIVE project is to design and test a low-power sensory readout and electronic interface. Originally, the deliverable prescribes thinning of the chip for flexibility. However, we assessed it not to be necessary to thin the chips for the following reasons: a) the chip area is small enough such that the chip's rigidity does not hamper it being mounted on a surface with a large radius of curvature (such as robotic fingertips), and b) the on-chip integrated sensors have a serious chance of being damaged during the thinning process.

In the second reporting period, to obtain the optimum readout architecture, a comparison study between a frame- and a spike-based readout was evaluated, in terms of its system power consumption and its texture recognition accuracy. Results from this modeling have been published in IEEE BioCAS 2022 [1]. Guided by the results of the study, a spike-based readout was considered to be the optimum choice. Consequently, the design and layout of a state-of-the-art spike-based per-taxel CMOS-based readout integrated circuit have been performed in a 0.18μm CMOS process. The chip has successfully been characterized and its performance metrics have been measured at KU Leuven. Furthermore, the readout chip has been post-processed at INTUITIVE partner Fondazione Bruno Kessler to integrate a per-taxel polyvinylidene fluoride (PVDF)-based piezoelectric sensor with a state-of-the-art 200μm spatial resolution, comparable to touch in human fingertips. A key innovation throughout this work is the integration on chip of a 12×16 taxel array with a per-taxel signal conditioning frontend and spiking readout combined with embedded neuromorphic first-order processing through Complex Receptive Fields (CRFs). The measurement results of this INTUITIVE e-skin readout chip have been accepted for publication in the 2023 Symposium on VLSI Technology and Circuits.

1. Modelling the optimum readout solution: frame- versus spike-based comparison

Addressing the need for a fast sensor array scan rate (1-10 kHz) required to detect fine tactile spatiotemporal stimuli [2], polling *e*-skin sensors in each array either sequentially [3][4] or in a column-based fashion [2][5]. The traditional readout process involves multiplexing the analog sensor output onto a central ADC for conversion, producing synchronous frames of tactile information, that are periodically transmitted for processing (see Fig. 1a). This periodic sensing and transmission of tactile frames, however, is power-inefficient, despite the fact that tactile stimuli may be sparse. Additionally, as the sensor count increases for future high-density e-skins, faster sensor polling rates are needed to achieve the necessary scan rate.

In contrast to the above conventional frame-based e-skin readouts, the ESR's research in INTUITIVE explores the use of neuromorphic, spike-based e-skin readout circuits. This approach differs from previously studied spiking e-skins where the sensor-to-spike conversion is performed in software [6][7][8] after ADC acquisition (see Fig. 1b). Instead, the proposed approach models a high-density e-skin readout with on-chip, taxel-wise sensor-to-spike conversion, leading to a more power-efficient design (see Fig. 1c).

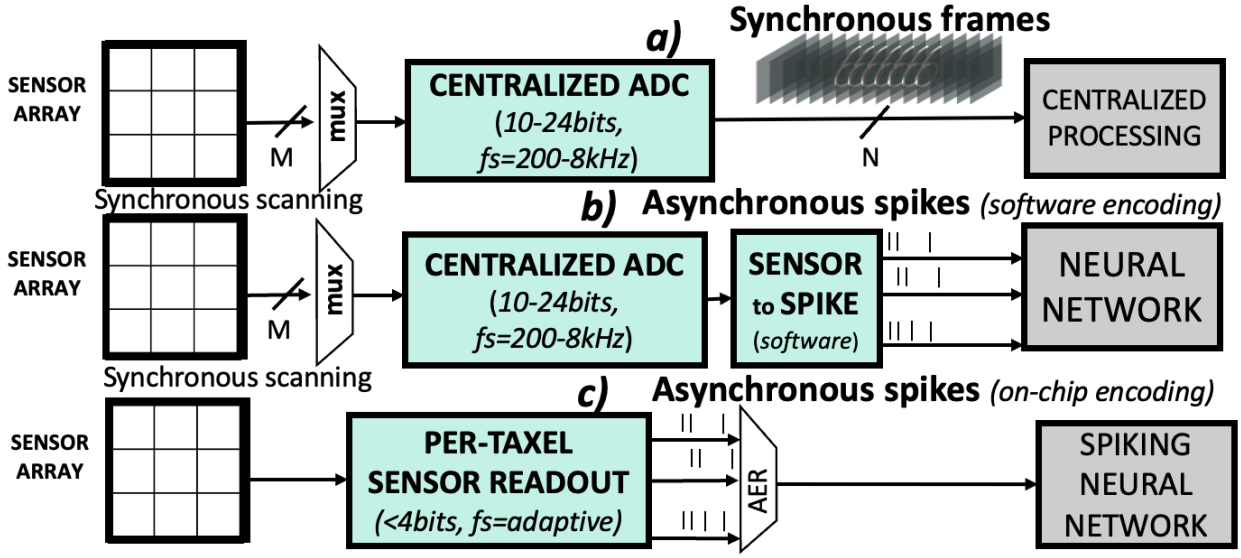


Fig.1. State-of-the-art electronic skin readout solutions can be classified in two major categories: (a) synchronous frame generation using a central ADC and further digital processing; (b) asynchronous spike generation in software followed by a neural network; and (c) on-chip, taxel-wise sensor-to-spike conversion connected directly to a spiking neural network.

Based on the system power consumption model developed in this research, we have shown that a spike-based readout is a power-optimal solution for the texture-sensing *e*-skin chip we are developing, as will be discussed in further detail in the next sections.

1.1. Taxel circuit architectures

1.1.1 Conventional level-crossing sampling

Previous research in dynamic vision sensors [9] has demonstrated that event-based sensing of time-sparse input signals contributes to more power-efficient readout electronics, which is critical when the sensor count continues to rise. Moreover, the deployment of individual taxels that respond independently to tactile stimuli, results in an efficient scaling between the actual information conveyed by the stimuli and the data transmission rate at the sensor output [10]. This asynchronous sampling of the signal allows the sampling of very fast transient changes on the tactile stimulus, common in texture scanning. Thus, straightforward *Level-Crossing Sampling* (LCS) converters [11] have been utilized for converting input signals into event-based spike trains. As illustrated in Fig. 2, the LCS converter generates a *spike* sample every time the input exceeds a predefined threshold away from the current value. The sequence of level crossings across numerous taxels is subsequently encoded as a series of taxel addresses, using an Address Event Representation (AER) interface.

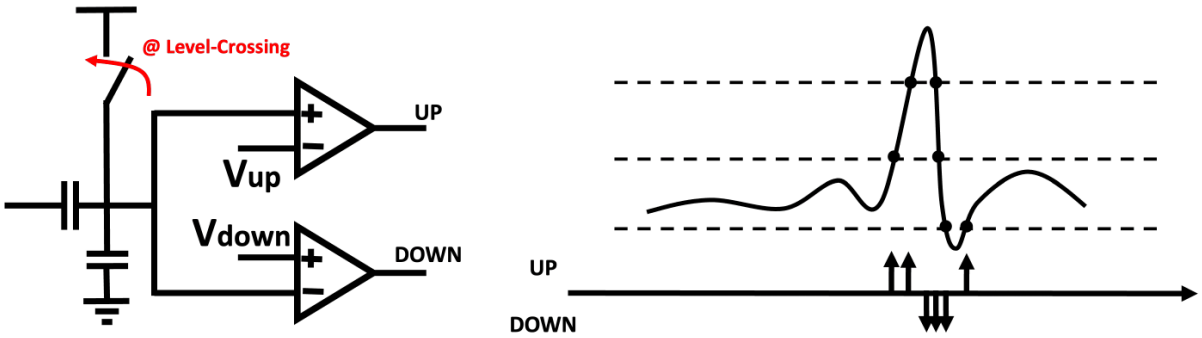


Figure 2. Analog to spike conversion using a non-uniform sampling/level-crossing converter.

A significant drawback of previously proposed LCS designs is the absence of level crossings during slow-moving inputs. This is because LCS converters are intended to detect signal changes, rather than the DC component. For time-sparse signals, the lack of level crossings results in a decreased signal conversion accuracy. Increasing the ADC resolution *N* to detect small signal changes, however, results in a power consumption increase with approximately a factor 2^{2N} [12]. Therefore, solutions, such as adding a triangular dither [13] or an adaptive threshold [14], have been explored to address this problem.

1.1.2 Neuromorphic level-crossing sampling

We presented a novel approach to addressing the issue of sampling slow tactile inputs by drawing on insights from neural encoding. Instead of using a *step-wise* decreasing threshold, as common LCS circuits do, we propose the use of an *exponentially-decaying* threshold as a more accurate model for biological neural encoding [15][16]. Fig. 3. compares our proposed *exponentially-decaying* threshold to the common *step-wise* dynamics.

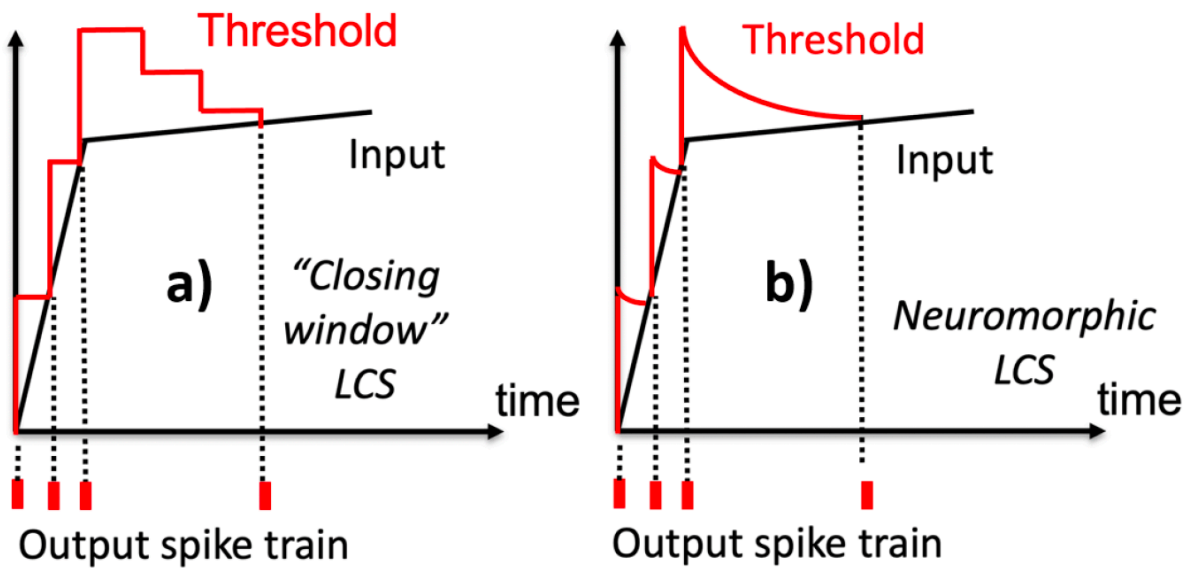


Figure 3. The closing window level-crossing sampling in a) approximates how a leaky neuron in b) generates spikes.

1.2. Power consumption analysis

To compare our event-based readout techniques with the frame-based approach in a multi-channel scenario, we have developed detailed power consumption models for the following readout circuits: *i)* spiking readout using regular LCS taxels without a closing window; *ii)* spiking readout using the proposed *neuromorphic* LCS taxels; and *iii)* a conventional frame-based readout with sensors multiplexed into a single ADC, with a typical figure of merit of approximately 10fJ per conversion step. Figure 4 provides a graphical representation of these models, assuming a 64-taxel array, which is consistent with the size of current state-of-the-art large-area e-skins. For small sensor signals with high output impedance, such as the piezoelectric sensors used in this work, an analog front-end (AFE) with gain and signal conditioning is needed.

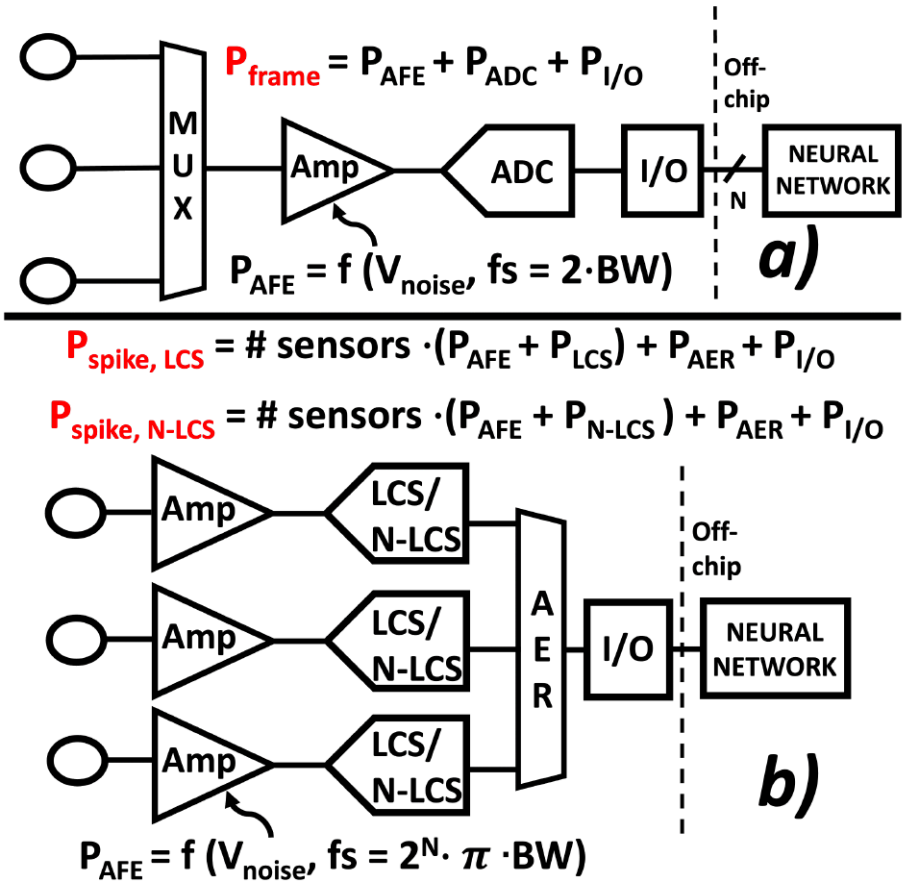


Figure 4. Blocks considered for power consumption modelling: in contrast to the frame-based readout in a), where the analog front-end (AFE) circuit is shared among all sensors, the spike-based readout in b) does require one AFE per taxel.

The power consumption analysis presented in Fig. 5 reveals important findings. Specifically, at low signal-to-noise ratio (SNR) (right bars in Fig. 5), the multi-channel spike-based readout is more power-efficient than the conventional frame-based counterpart, consistent with previous single-channel analysis that did not account for the AFE power consumption [12]. However, at high SNR (left bars in Fig. 5), the power consumption of the per-taxel AFE in spike-based readouts becomes dominant, rendering the spike-based solution less power-efficient compared to the frame-based counterpart, despite the lower transmission power resulting from the compressive transfer of spiking data.

Thus, we conclude that the spike-based readout is most suitable in challenging signal acquisition scenarios where the input SNR is low. We maintain that this is applicable to our e-skin chip for texture sensing, where noisy output spikes are characteristic for the biological systems we are

emulating, and can effectively be handled by biological and artificial spiking neural networks (SNNs) without much loss in the accuracy.

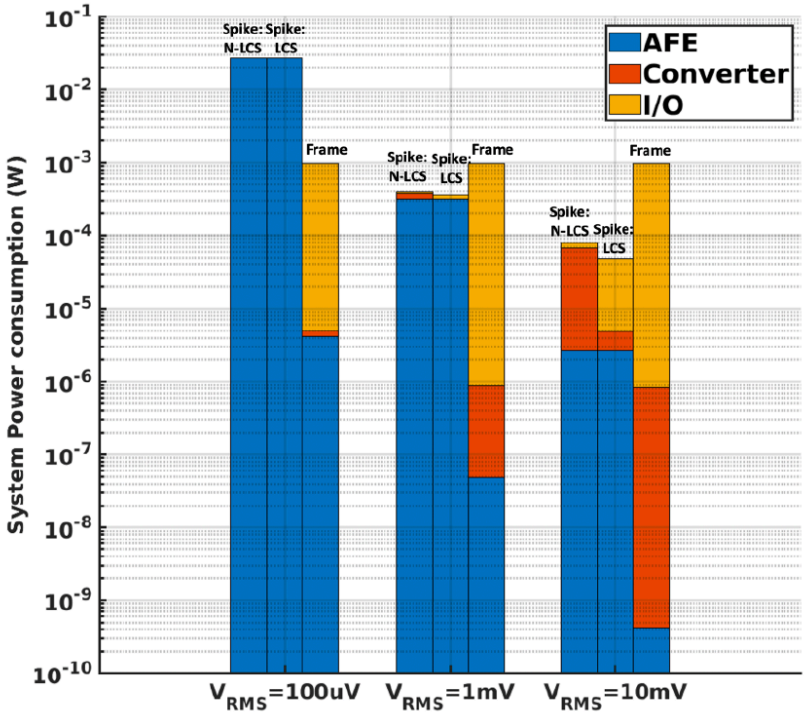


Figure 5. System power consumption breakdown for spike- and frame-based readouts, at three different AFE noise RMS target.

2. Spiking readout circuit design

2.1. System architecture and taxel circuits

The designed taxel readout chip (see the chip photo in Fig. 6) features 12×16 taxels with two spiking readout channels each (see the schematic in Fig. 7(a)): a voltage-mode level-crossing sampling (LCS) and a neuromorphic current-mode LCS (N-LCS) converter readout. The dual readout channel design allows for flexibility in the spike generation depending on the application (robotics, neuroprosthetics, etc.). For robotics applications, existing SNN hardware and algorithms have been developed more commonly for pure threshold-based spiking input (without adaptation). Meanwhile, for neuroprostheses, the neuron-like nature of the output spike generation (with adaptation) could result in more biologically-faithful spike-based tactile sensing.

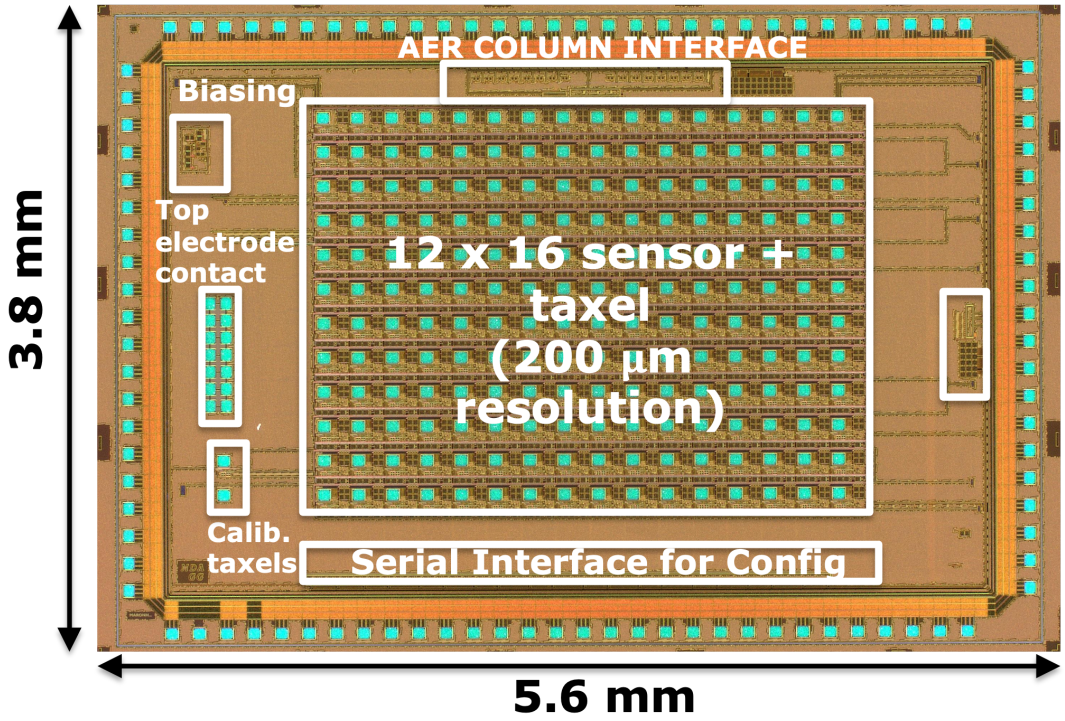


Figure 6. Photo of the INTUITIVE e-skin readout chip consisting of 12x16 taxels with state-of-the-art 200-µm spatial resolution. Each sensor is connected to two spiking readout channels. Throught the Address Event Representation (AER) interface, the output spikes are encoded into asynchronous bursts of individual taxel addresses to form a spike train.

The per-taxel piezoelectric sensor charge output is converted to a voltage input for the LCS channel, while an extra voltage-to-current (V-I) stage is used to generate current inputs for the N-LCS. The voltage input then goes into two window comparators to detect bipolar level crossings, as seen in Fig. 2. Meanwhile, the N-LCS outputs unipolar spikes through a delta modulator. The N-LCS operates in the current-mode domain, since ultra-low power, synaptic-like current-mode low-pass filters can be designed with minimal circuit complexity. The N-LCS's output spikes are integrated through two low-pass filters (with fast and slow time constants), forming an exponentially decaying threshold for spiking, just like in biological spike encoding.

The per-taxel signal conditioning circuit contains a charge amplifier with configurable charge gain and sub-1Hz high-pass corner frequency, and a low-area, tunable V-I converter for the N-LCS channel. To achieve low power consumption, the analog circuits are biased in the subthreshold region with VDD=1V, along with the taxel digital blocks and the AER interface. The encoding parameters (for LCS & N-LCS), such as the spiking threshold and the decay time constant, can be configured from off-chip, allowing for software-based flexibility on the spike generation. A chip micrograph of the dual-channel per-taxel spiking readout layout with 200 x 200 μm^2 area is shown in Fig. 7b.

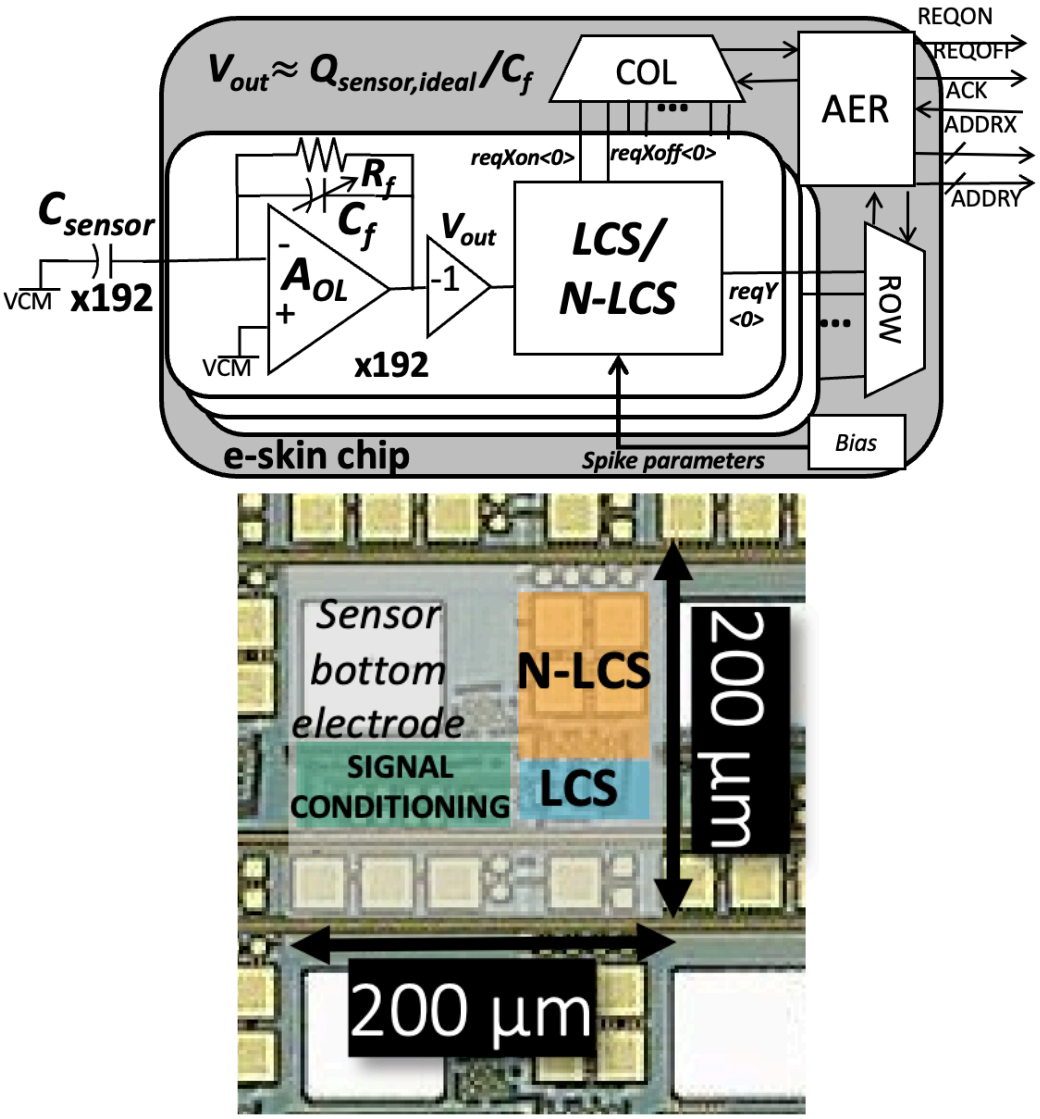


Figure 7. (a) The per-taxel readout circuitry consists of a signal conditioning front-end with configurable closed-loop gain, an ultra-low-current voltage-to-current converter for the N-LCS channel, a voltage-mode level-crossing sampling (LCS) channel, and a neuromorphic current-mode LCS channel. The level crossings are transmitted to the on-chip AER interface through a per-taxel digital logic circuit. (b) The dual readout channel layout is shown, occupying 200 x 200 μm^2 per taxel, the smallest compared to the the state of the art.

3. Sensor deposition

3.1. Wafer post-processing

A 12x16 piezoelectric sensor array has been integrated directly on top of the CMOS readout chip, resulting in a 1:1 sensor-to-spiking readout ratio, which is a first in *e*-skin designs. The wafer-based post-processing step has been performed at Fondazione Bruno Kessler (FBK). The sensor cross-section, including the input PMOS of the per-taxel readout, is shown in Fig. 8a. The chip micrograph of the post-processed chip is shown in Fig. 8b, clearly showing the patterned Au + PVDF layer on top of the CMOS chip.

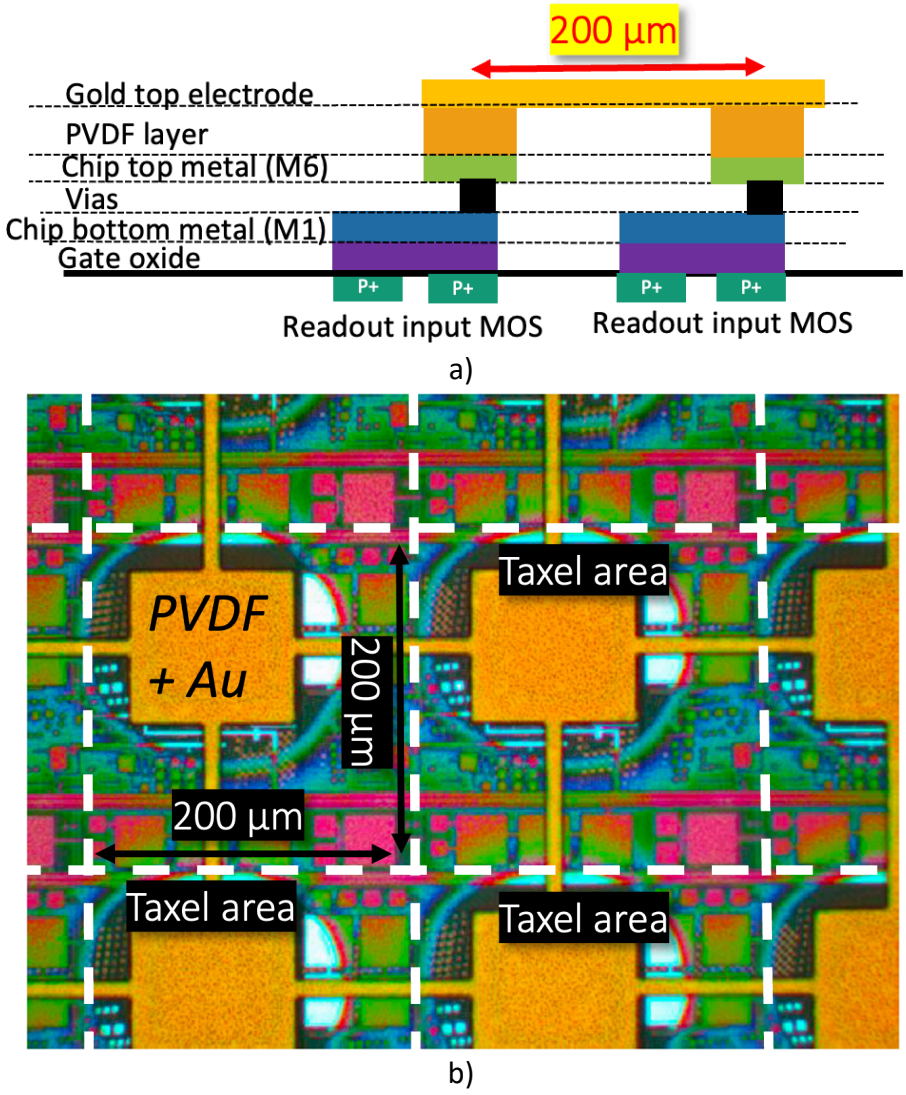


Figure 8. Wafer-based sensor post-processing: a) cross-sectional description of the CMOS + sensor stack; b) chip micrograph showing the taxels of the post-processed readout chip

To form the bottom electrode of an individual sensor, which connects to the per-taxel readout, a pad consisting of an un-passivated 75x75-µm^2 sheet of CMOS top metal is instantiated. A PVDF solution of PVDF-TrFE (Piezotech FC20) was spin-coated on a 73 x 67.5-mm^2 piece of the 8" wafer.

The top electrode (Au) is deposited through sputtering and is then patterned. The patterned Au top electrode also serves as a mask during PVDF patterning through dry etching. The top electrode is connected to the CMOS chip by manually dropping a small conductive epoxy ball on the intersection of the left-most edge of the top electrode and a pad array (Fig. 9). This is a clever approach to connecting the top electrode without a) wirebonding a pad directly to the top electrode, and b) adding another via or patterned metal layer that increases the number of masks and processing steps. To de-risk the sensor post-processing to be performed on the readout chips from the 8" wafers, sensor test structures were first developed on FBK 6" wafers.

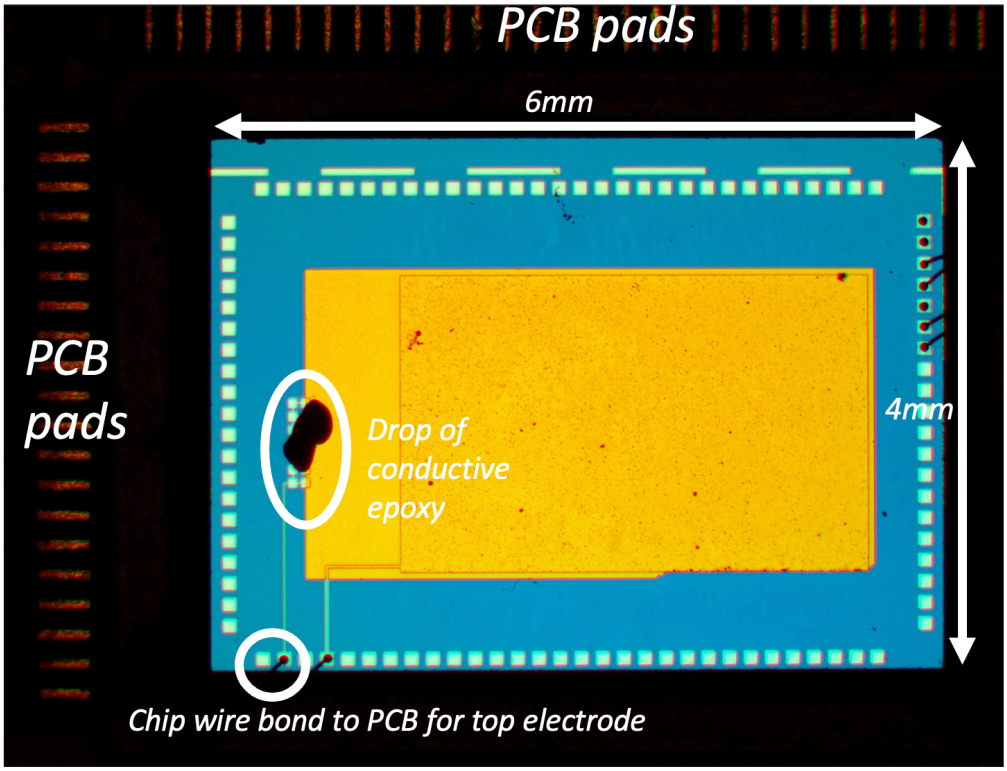


Figure 9. To connect the top electrode to a known potential for sensor biasing, a setup is proposed wherein the intersection of a group of pads and the edge of the top electrode can be connected electrically with a conductive epoxy. The image depicts wirebonding on the test structure chips from 6" wafers.

The thick passivation layers of the wafer could present an issue when aiming to deposit a 250-nm layer of PVDF, possibly resulting in large variations in the sensor thickness. To improve the PVDF thickness uniformity, an 8" wafer has undergone a chemo-mechanical polishing (CMP) step, with the aim of reducing the passivation step. The CMP step, however, proved to be damaging to also the chip top metal (Fig. 10b). Therefore, the targeted passivation thickness reduction was not achieved. The resulting change in the passivation step profile (Fig. 10c & 10d) is revealed through mechanical profilometry (Fig. 10a).

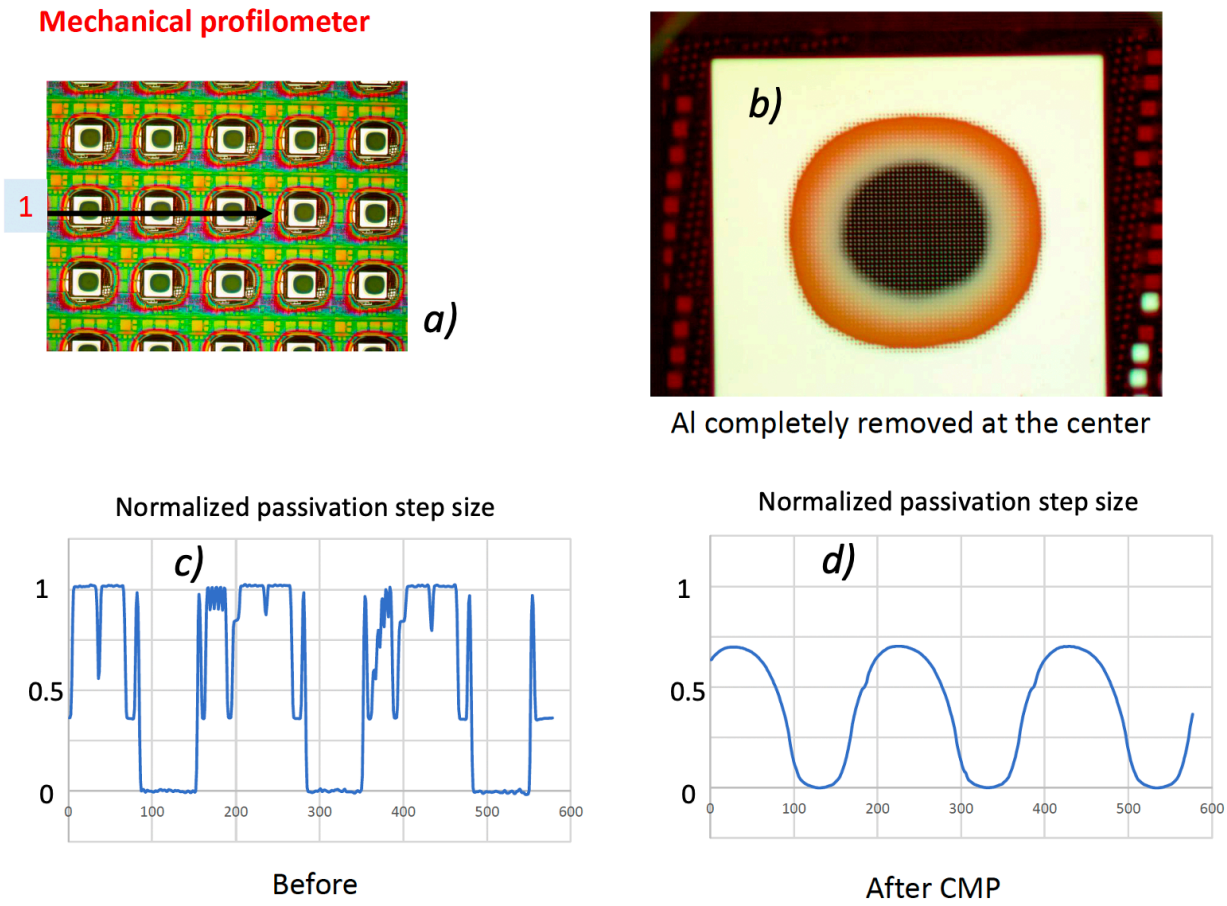
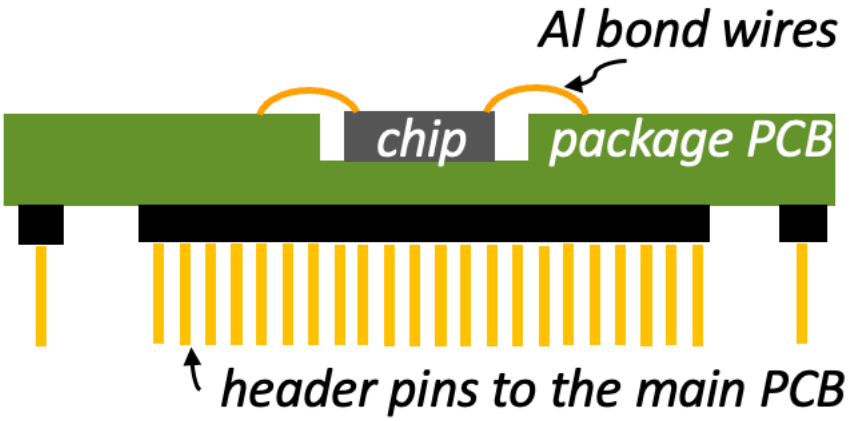


Figure 10. a) A mechanical profilometer is scanned across the chip electrodes to characterize the passivation step profile post-CMP; b) the CMP procedure etched parts of the Al electrodes as well, resulting in an incomplete etching of the passivation layers. The passivation profile of the scanned area in a) at c) pre-CMP and d) post-CMP.

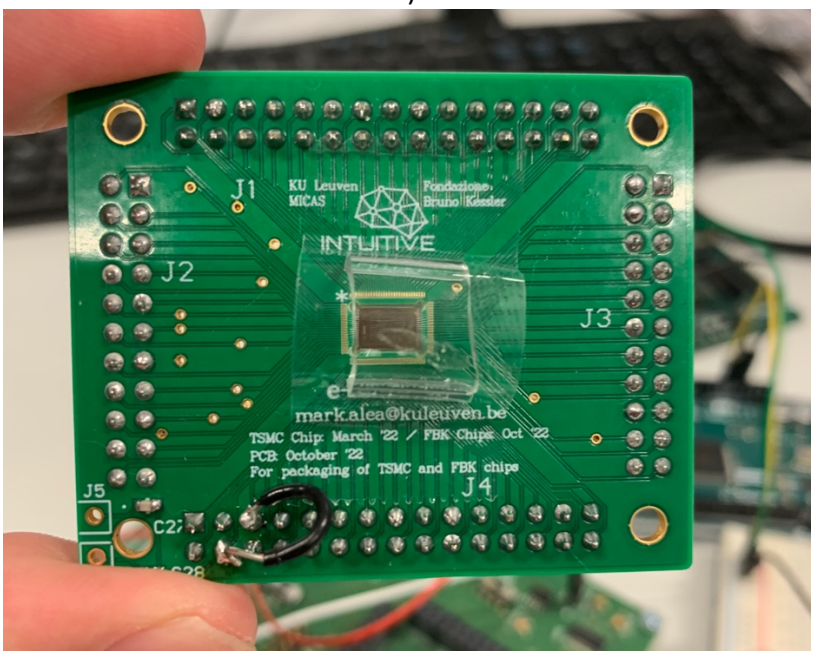
4. Chip packaging and test measurement set-up

4.1. Chip wire bonding

A key consideration in the chip wire bonding (electrical connection of the chip to off-chip circuits through the packaging PCB) is to make them more robust to external mechanical forces during texture scanning or any other form of force contact. This is accomplished by reducing the heights of the Al bond pads that connect the chip to the PCB pads (Fig. 11a). To do this, an 800-µm cavity is cut out of the packaging PCB, which is the same thickness as the chips. This allows for the top surfaces of both the chip and the PCB to align, allowing for shorted Al bondwires and lower bondwire heights. The packaged PCB is shown in Fig. 11b.



a)



b)

Figure 11. a) To reduce the chip bondwires for increased robustness during mechanical contact, the area where the chip is to be bonded to the package PCB is milled by 0.8 mm (same chip thickness). b) Image showing the actual readout chip bonded on the package PCB. The chip contains 100 pads in total: 52 (optional external AER interface), VDDPST-5V (2), VDD-1.8V (2), AVDD-1V (2), LCVDD-1V (1), DVDD-1V (2), GND (5), AER interface (12) , serial interface (4), current biasing (1), voltage biasing (2), spike generation parameters (8), analog output for debug (2), calibration (2), digital configuration bits (2), and poling mode enable (1).

4.2. Test measurement setup

To facilitate chip measurements and characterization, a PCB test board (Fig. 12) has been designed and fabricated. The test board consists of internal power generation derived from a 5V supply (1.8 V & 1 V output), internal voltage, and current bias generation for both circuit biasing

and spiking parameter configuration. Output spikes are recorded by an Arduino MEGA2560 off-chip through the AER interface headers. An optional off-chip AER interface and control is also possible by disabling the internal AER blocks. A 16-channel voltage DAC is used to apply input to the readout chip, emulating the sensor charge response, appropriately scaled to reflect the sensor capacitance and readout open-loop gain.

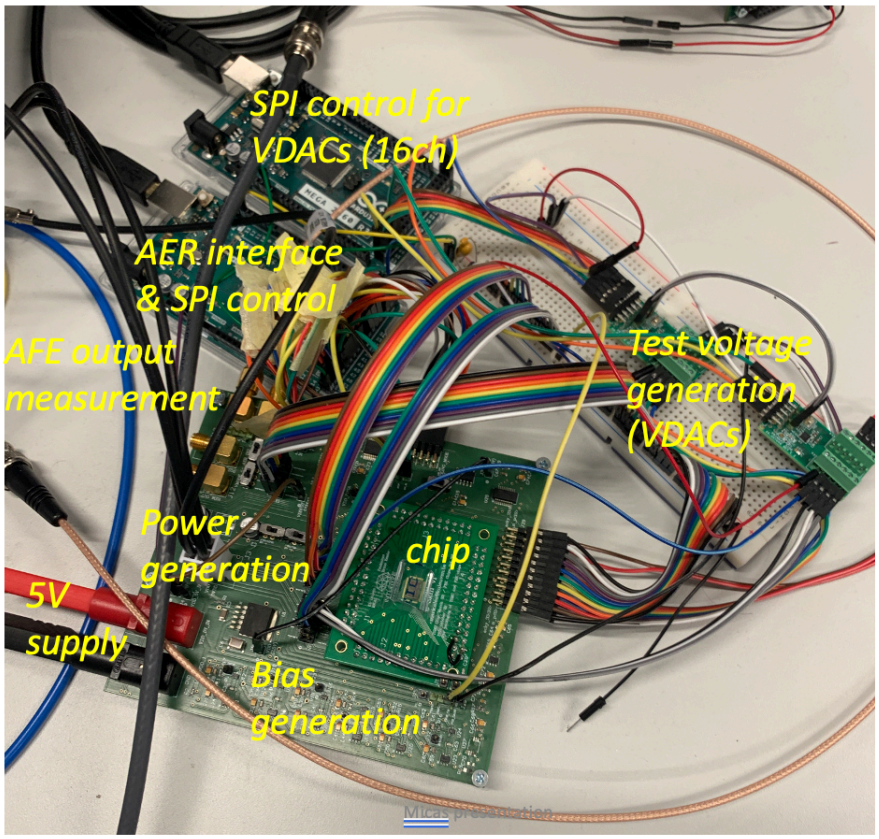


Figure 12. Photo showing the test measurement setup.

5. Chip measurements

5.1. Texture scan

In this section, we simulate a texture scan with the readout chip and measure the chip's response through its output spikes. Due to the lack of publicly-available multi-sensor tactile-based texture datasets, we developed a technique to emulate sensor signal generation during a multi-sensor texture scan (see Fig. 13). To model the piezoelectric sensor array response when scanning a texture, a 12x16 array of time-series texture signals is generated from texture images [17]. The voltage signals, scaled to reflect the sensor charge output, are then fed as input to 16 channels of the chip (limited by the chip bond pads available for connection). The output spikes coming from the on-chip AER interface are then recorded off-chip. The spike addresses are then

sequentially re-mapped such that it mimics how an actual tactile stimulus encounters the chip's 12×16 taxels. An example spatiotemporal depiction of the output spikes is shown in Fig. 13. The generated texture spike dataset is available online at: tinyurl.com/kyltexture.

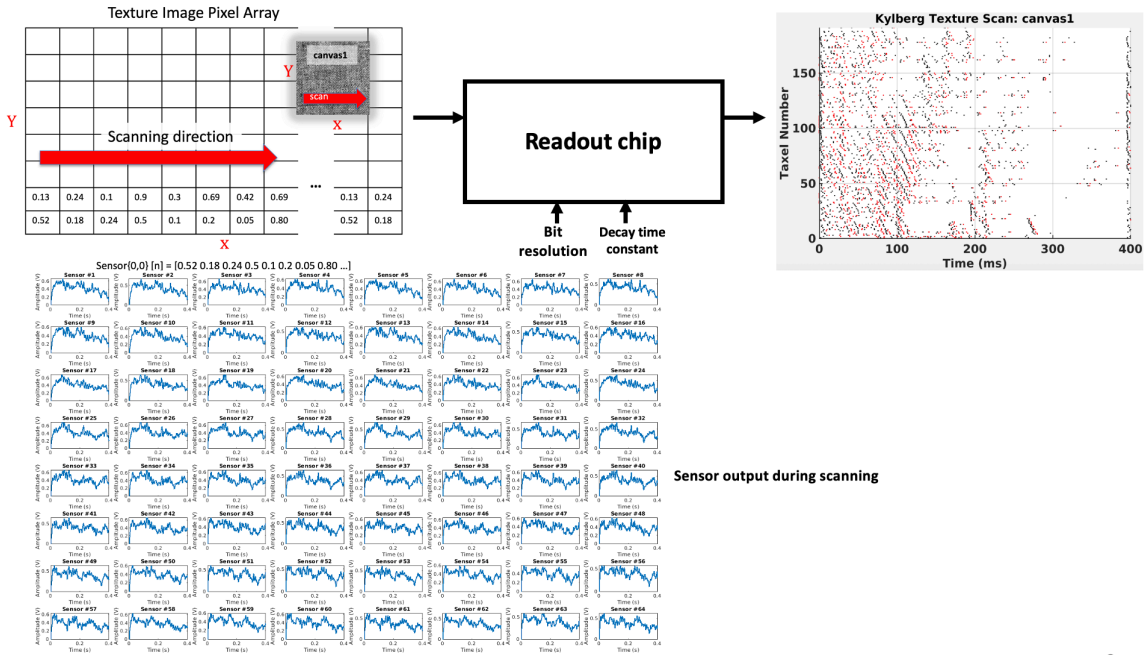


Figure 13. Methodology to simulate an ideal texture scan to generate the texture spiking dataset

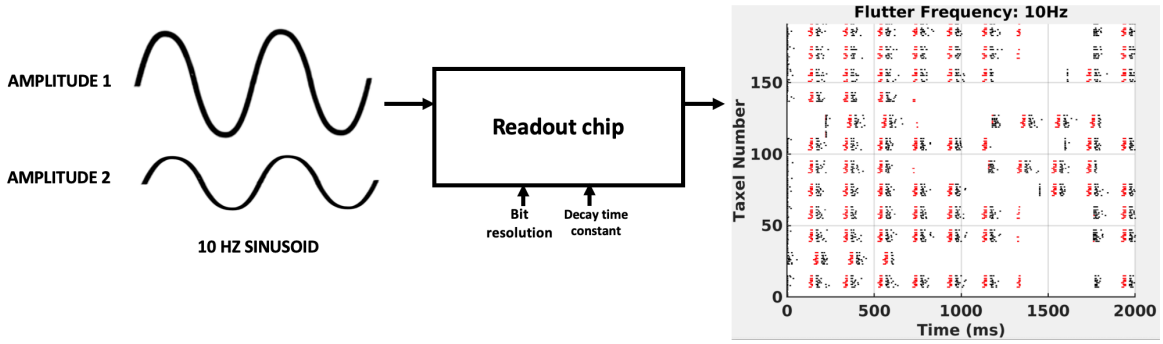


Figure 14. Vibration in the flutter frequency range is used as input for the chip

5.2. Flutter frequency classification

Humans have been known to be very sensitive to low-frequency vibration (*i.e.* flutter) [18]. In this section, we prove that our e-skin readout chip is equally adept at perceiving and classifying flutter vibrations by subjecting the e-skin readout chip to low-frequency sinusoidal inputs (0.5 to 15 Hz). To demonstrate amplitude invariance, we used two different signal amplitudes. The output

spikes for a 10-Hz flutter frequency input are shown in Fig. 14. The generated texture spike dataset is available online at: *tinyurl.com/flutter6.*

5.3. Measured power consumption

The chip's power consumption has been characterized at two conditions, as summarized in Table I : 1) in standby mode (no events), and 2) at a moderate event rate of 62500 events/second. The chip consumes very low power in standby mode, and is dominated by the leakage of the digital output buffers for the AER interface. For proper interfacing, the 1-V output of the internal AER interface is first level-shifted to 1.8V and then to 5V for compatibility with common commercial I/O interfaces. The per-taxel power consumption, dominated by the signal conditioning frontend power consumption, is not dependent on the event rate. The scalability of the chip's power consumption on the event rate highlights the benefits of the event-driven nature of the sensor acquisition that we have proposed in this research.

Table I. INTUITIVE e-skin readout chip's measured power consumption.

Events per second	**Power consumption**				
	Chip (total)	Core (taxels + AER)	I/O (1.8V & 5V logic)	Per-taxel (LCS)	Per-taxel (N-LCS)
0 (standby)	0.075 mW	0.052 mW	0.023 mW	12 nW	53 nW
62500	5.09 mW	5.06 mW	0.03 mW		

5.4. Comparison to state-of-the-art

Compared to prior e-skin results (see Table II), this work achieves around 100-7000X reduction in the system power consumption and more than 5 orders of magnitude reduction in the per-taxel power consumption, while enhancing the spatial resolution by 5X and doubling the sensor count. The per-taxel sensor frontend design achieves state-of-the-art performance in the charge resolution (270X reduction), area (10X smaller), and power consumption (> 30X lower), while having the most (192) channels integrated on chip (see Table III). Lastly, the system achieves a state-of-the-art classification accuracy despite using a small SNN network without preprocessing, a low equivalent spike encoding resolution (3 to 4 bits), and a low data rate (< 2.2 kHz).

Table II. Comparison to state-of-the-art e-skins with tactile stimuli classification.

	SCI.ROBOT19 [2]	TBCAS 18 [3]	SENSORS 22[11]	JNN20 [12]	This work
Sensors	Piezoresistive	Piezo-resistive	Piezo-resistive	MEMS	**Piezoelectric**
# of Sensors	80	6	9	4	**192**
Spatial Res.	> 1 mm	1 mm	2.5 mm	-	**0.2 mm**
Power consumption	*System:* 560mW *Per-taxel*: 7mW	-	-	*Readout*: 42 mW	***System:* 75µW to 5.09mW[a]** ***LCS/N-LCS:* 12.33/53nW**
Supply	3.3V	3.3V	-	5V	**Taxel + AER: 1V, I/O: 5V**
Sensor data	Spikes	Spikes	Spikes	Spikes	**Spikes (on-chip)**
ADC Res.	10b	12b	10b	24b	**3-4b**
Acquisition Datarate[b]	8 MHz (parallel)	21.6 kHz (sequential)	130 kHz (parallel)	146 kHz (parallel)	**<2.235 kHz[c] (event-driven, spike rate)**
Classifier	KNN, MLP	ELM	SVM	SNN + KNN	**SNN + Linear SVM**
Preprocessing	ISI	None	ISI	None	**None**
Classification Accuracy	Curvature (3-class): **97%**; Grating(6-class): **88%**	Texture (10-class): **92%**	Texture (13-class): **97.12%**	Texture (10-class): **94.2%**	Texture (6-class)[d]: **97.0833%** Flutter (6-class)[de]: **99.1667%;**

[a]0 to 62.5k event/s [b]DR=#bits*fsample*#sensors [c]Texture scan (192 taxels) [d]model sensor input [e]amplitude-invariant

Table III. Comparison to state-of-the-art PVDF-based signal conditioning frontends

	TBCAS19 [13]	ISCAS20 [14]	SENSORS17 [15]	This work
Technology	0.13µm	65nm	COTS	**0.18µm**
Min. charge	0.1 pC	0.1 pC	0.15 pC	**0.00037 pC[a]**
# of AFE ch.	13	1	2	**192**
Power / ch. (µW)	7 (2.5V)	0.112(2.5V)	7000 (5V)	**0.003[b] (1V)**
Area / ch. (mm²)	0.24	0.0277	-	**0.0027**
CRFs	No	No	No	**Yes**

[a]input-referred noise (Csensor=172fF; 1 to 10kHz BW); [b]simulated (VMODE)

6. Conclusion

In conclusion, this research has compared frame-based and spike-based readout solutions for electronic skin (e-skin) tactile sensors. The traditional frame-based readout involves multiplexing the analog sensor output onto a central ADC, resulting in a periodic transmission of tactile frames, which is power-inefficient. In contrast, the spike-based readout utilizes neuromorphic, on-chip, taxel-wise sensor-to-spike conversion, leading to a more power-efficient design. The research has developed power consumption models and has analyzed the power efficiency of both approaches. The findings indicate that spike-based readout is more power-efficient than frame-based readout at low signal-to-noise ratios, making it suitable for signal acquisition scenarios with low input SNR. The proposed spike-based readout solution is most applicable to e-skin chips for texture sensing, where noisy output spikes can effectively be handled by artificial spiking neural networks without significant loss in accuracy.

This work is the first demonstration on chip of end-to-end e-skin sensor-to-spike encoding with embedded CRF processing at fingertip-mimicking high taxel density. The e-skin taxel readout chip has been implemented in a 0.18-µm CMOS technology. It achieves the highest reported spatial resolution of 200 µm, comparable to human fingertips. A key innovation is the integration on chip of a 12×16 taxel array with a per-taxel signal conditioning frontend and spiking readout combined with embedded neuromorphic first-order processing through Complex Receptive Fields (CRFs). Experimental results have shown that spiking neural network (SNN)-based classification of the chip's spatiotemporal spiking output for input tactile stimuli such as texture and flutter frequency, achieves excellent accuracies up to 97.1% and 99.2% of classification accuracy, respectively. Note that this is despite using only a small 256-neuron SNN classifier, a low equivalent spike encoding resolution of 3-4 bits, a sub-Nyquist 2.2-kHz population spiking rate, and a state-of-the-art per-taxel (12.33 nW) and per-system (75 µW -5 mW) power consumption.

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