

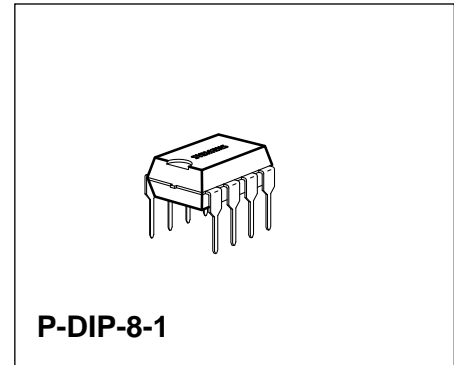
## Control IC for Switched-Mode Power Supplies using MOS-Transistors

TDA 4605

Bipolar IC

### Features

- Fold-back characteristic provides overload protection for external components
- Burst operation under short-circuit conditions
- Loop error protection
- Switch-off if line voltage is too low (undervoltage switch-off)
- Line voltage compensation of overload point
- Soft-start for quiet start-up
- Chip-over temperature protection (thermal shutdown)
- On-chip parasitic transformer oscillation suppression circuitry



Type	Ordering Code	Package
TDA 4605	Q67000-A8078	P-DIP-8-1

The IC TDA 4605-1 controls the MOS-power transistor and performs all necessary regulation and monitoring functions in free running flyback converters. Since good load regulation over a wide load range is attained, this IC is applicable for consumer and industrial power supplies.

The serial circuit of power transistor and primary winding of the flyback transformer is connected to the input voltage. During the switch - on period of the transistor, energy is stored in the transformer and during the switch - off period it is fed to the load via the secondary winding. By varying switch-on time of the power transistor, the IC controls each portion of energy transferred to the secondary side such that the output voltage remains nearly independent of load variations.

The required control information is taken from the input voltage during the switch-on period and from a regulation winding during the switch-off period.

In the different load ranges the switched-mode power supply (SMPS) behaves as follow:

**No load operation:**

The power supply unit oscillates at its resonant frequency typ. 100 kHz to 200 kHz. Depending upon the transformer windings the output voltage can be slightly above nominal value.

**Nominal operation:**

The switching frequency declines with increasing load and decreasing AC-voltage. The duty factor primarily depends on the AC-voltage. The output voltage is load-dependent only.

**Overload point:**

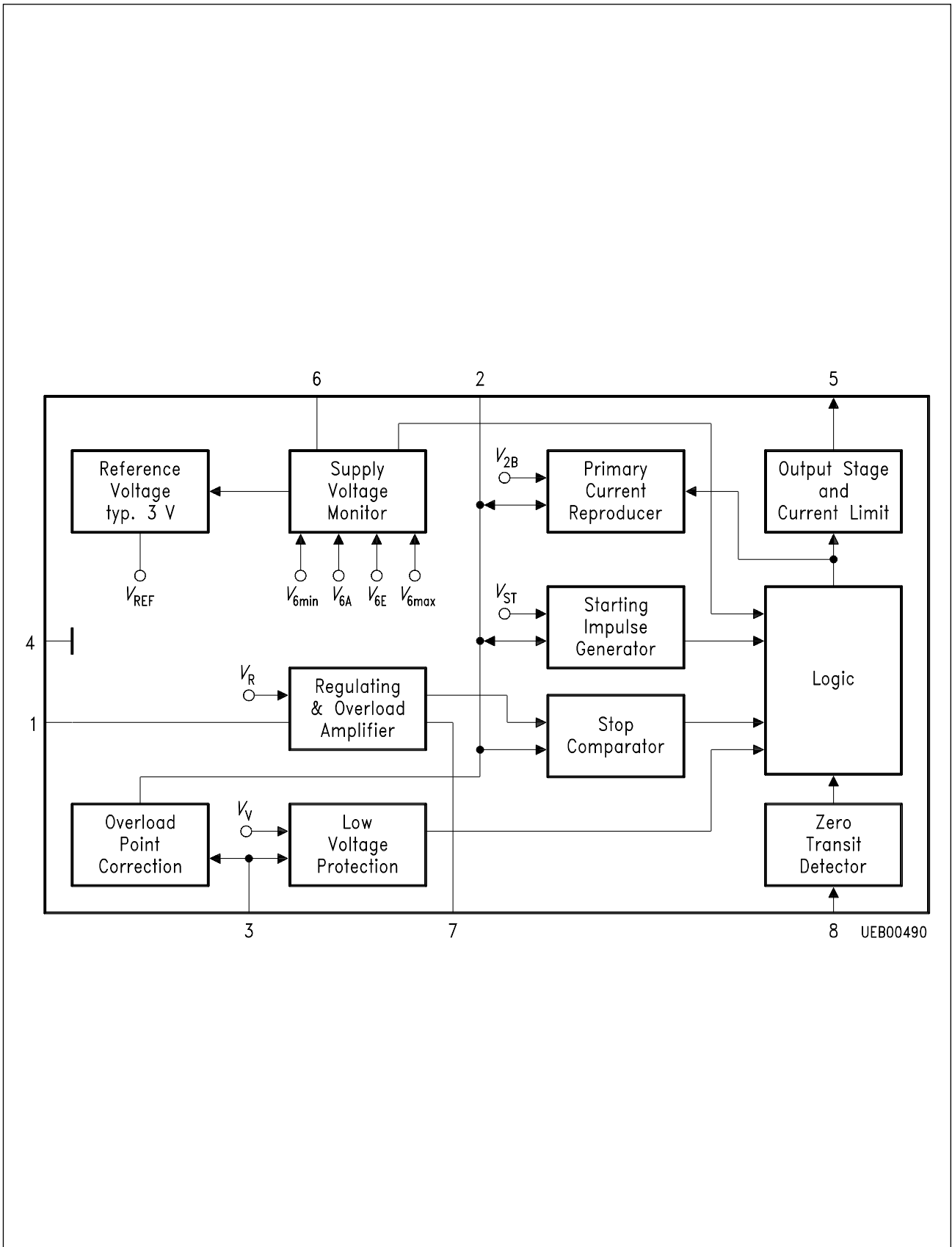
Maximal output power is available at this point of the output characteristic.

**Overload:**

The energy transferred per operation cycle is limited at the top. Therefore the output voltage declines by secondary overloading.

## Pin Definitions and Functions

Pin No.	Function
1	<b>Regulating Voltage:</b> Information input concerning secondary voltage. By comparing the regulating voltage - obtained from the regulating winding of the transformer - with the internal reference voltage, the output impulse width on pin 5 is adapted to the load of the secondary side (normal, overload, short-circuit, no load).
2	<b>Primary Current Simulation:</b> Information input regarding the primary current. The primary current rise in the primary winding is simulated at pin 2 as a voltage rise by means of external RC-element. When a value is reached that is derived from the regulating voltage at pin 1, the output impulse at pin 5 is terminated. The RC-element serves to set the maximum power at the overload point set.
3	<b>Input for Primary Voltage Monitoring:</b> In the normal operation $V_3$ is moving between the thresholds $V_{3H}$ and $V_{3L}$ ( $V_{3H} > V_3 > V_{3L}$ ). $V_3 < V_{3L}$ : SMPS is switched OFF (line voltage too low). $V_3 > V_{3H}$ : Compensation of the overload point regulation (controlled by pin 2) starts at $V_{3H}$ : $V_{3L} = 1.7$ .
4	<b>Ground</b>
5	<b>Output:</b> Push-pull-output provides $\pm 1$ A for rapid charge and discharge of the gate capacitance of the power MOS-transistor.
6	<b>Supply Voltage Input:</b> A stable internal reference voltage $V_{REF}$ is derived from the supply voltage also the switching thresholds $V_{6A}$ , $V_{6E}$ , $V_{6\max}$ and $V_{6\min}$ for the supply voltage detector. If $V_6 > V_{6E}$ then $V_{REF}$ is switched on and switched off when $V_6 < V_{6A}$ . In addition the logic is only enable for $V_{6\min} < V_6 < V_{6\max}$ .
7	<b>Soft-Start:</b> Input for soft-start. Start-up will begin with short pulses by connecting a capacitor from pin 7 to ground.
8	<b>Zero Detector:</b> Input for the oscillation feedback. After starting oscillation, every zero transit of the feedback voltage (falling edge) triggers an output impulse at pin 5. The trigger threshold is at + 50 mV typical.



Block Diagram

## Circuit Description

### Application Circuit

Application circuit shows a flyback converter for video recorders with a power rating of 50 W. The circuit is designed as a wide-range power supply for AC-line voltages of 90 to 270 V. The AC-input voltage is rectified by bridge rectifier GR1 and smoothed by  $C_1$ . The NTC limits the rush in current.

In the period before the switch-on threshold is reached the IC is supplied via resistor  $R_1$ ; during the start-up phase it uses the energy stored in  $C_2$ , under steady-state conditions the IC receives its supply voltage from transformer winding  $n_1$  via diode D1. The switching transistor T1 is a BUZ 90. The parallel-connected capacitor  $C_3$  and the inductance of primary winding 112 determine the system resonance frequency. The  $R_2 - C_4 - D2$  circuitry limits overshoot peaks, and  $R_3$  protects the gate of T1 against static charges.

While T1 conducts, the current rise in the primary winding depends on the winding's inductance and the  $V_{C1}$  voltage. A voltage reproduction of the current rise is tapped using the  $R_4 - C_5$  network and forwarded into pin 2 of the IC. The RC-time constant of  $R_4$ ,  $R_5$  must be dimensioned correctly in order to prevent driving the transformer core into saturation.

The  $R_{10}/R_{11}$  divider ratio provides the line voltage threshold controlling the undervoltage control circuit in the IC. The voltage present at pin 3 also determines the overload. Detection of overload together with the current characteristic at pin 2 controls the on period of T1. This keeps the cut-off point stable even with higher AC-line voltages.

Regulation of the switched-mode power supply is via pin 1. The control voltage of winding  $n_1$  during the off-period of T1 is rectified by D3, smoothed by  $C_6$  and stepped down at an adjustable ratio by  $R_5$ ,  $R_6$  and  $R_7$ . The  $R_6 - C_7$  network suppresses parasitic overshoots (transformer oscillation). The peak voltage at pin 2, and thus the primary peak current, is adjusted by the IC so that the voltage applied across the control winding, and hence the output voltages, are at the desired level.

When the transformer has supplied its energy to the load, the control voltage passes through zero. The IC detects the zero crossing via series resistors  $R_9$  connected to pin 8. But zero crossings are also produced by transformer oscillation after T1 has turned off if output is short-circuited. Therefore the IC ignores zero crossings occurring within a specified period of time after T1 turn-off.

The capacitor  $C_8$  connected to pin 7 causes the power supply to be started with shorter pulses to keep the operating frequency outside the audible range during start-up.

On the secondary side, five output voltages are produced across winding  $n_3$  to  $n_7$  rectified by D4 to D8 and smoothed by  $C_9$  to  $C_{13}$ . Resistors  $R_{12}$ ,  $R_{14}$  and  $R_{19}$  to  $R_{21}$  are used as bleeder resistors. Fusible resistors  $R_{15}$  to  $R_{18}$  protect the rectifiers against short circuits in the output circuits, which are designed to supply only small loads.

## Block Diagram

### Pin 1

The regulating voltage forwarded to this pin is compared with a stable internal reference voltage  $V_R$  in the **regulating and overload amplifier**. The output of this stage is tied to the stop comparator.

### Pin 2

A voltage proportional to the drain current of the switching transistor is generated there by the external RC-combination in conjunction with the **primary current transducer**. The output of this transducer is controlled by the logic and referenced to the internal stable voltage  $V_{2B}$ . If the voltage  $V_2$  exceeds the output voltage of the regulating amplifier, the logic is reset by the stop comparator and consequently the output of pin 5 is switched to low potential. Further inputs for the logic stage are the output for the **start impulse generator** with the stable reference potential  $V_{ST}$  and the **supply voltage monitor**.

### Pin 3

The down-divide primary voltage applied there stabilizes the overload point. In addition the logic is disabled in the event of low voltage by comparison with the internal stable voltage  $V_V$  in the primary voltage monitor block.

### Pin 4

Ground

### Pin 5

In the output stage the output signals produced by the logic are shifted to a level suitable for MOS-power transistors.

### Pin 6

From the supply voltage  $V_6$  are derived a stable internal reference  $V_{REF}$  and the switching threshold  $V_{6A}$ ,  $V_{6E}$ ,  $V_{6\max}$  and  $V_{6\min}$  for the supply voltage monitor. All reference values ( $V_R$ ,  $V_{2B}$ ,  $V_{ST}$ ) are derived from  $V_{REF}$ . If  $V_6 > V_{VE}$  the  $V_{REF}$  is switched on and switched off when  $V_6 < V_{6A}$ . In addition, the logic is released only for  $V_{6\min} < V_6 < V_{6\max}$ .

### Pin 7

The output of the overload amplifier is connected to pin 7. A load on this output causes a reduction in maximal impulse duration. This function can be used to implement a soft start, when pin 7 is connected to ground by a capacitor.

## Pin 8

The zero detector controlling the logic block recognizes the transformer being discharged by positive to negative zero crossing of pin 8 voltage and enables the logic for a new pulse. Parasitic oscillations occurring at the end of a pulse cannot lead to a new pulse (double-pulsing), because an internal circuit inhibits the zero detector for a finite time  $t_{UL}$  after the end of each pulse.

## Start-Up Behaviour

The start-up behaviour of the application circuit per sheet 48 is represented on sheet 50 for a line voltage barely above the lower acceptable limit voltage value (without soft-start). After applying the line voltage at the time  $t_0$  to the following voltages built up:

- $V_6$  corresponding to the half-wave charge current over  $R_1$
- $V_2$  to  $V_{2\max}$  (typically 6.6 V)
- $V_3$  to the value determined by the divider  $R_{10}/R_{11}$ .

The current drawn by the IC in this case is less than 1.6 mA. If  $V_6$  reaches the threshold  $V_{6E}$  (time point  $t_1$ ), the IC switches on the internal reference voltage. The current draw max. rises to 12 mA. The primary current- voltage reproducer regulates  $V_2$  down to  $V_{2E}$  and the starting impulse generator generates the starting impulses from time point  $t_5$  to  $t_6$ . The feedback to pin 8 starts the next impulse and so on. All impulses including the starting impulse are controlled in width by regulating voltage of pin 1. When switching on this corresponds to a short-circuit event, i.e.  $V_1 = 0$ . Hence the IC starts up with "short-circuit impulses" to assume a width depending on the regulating voltage feedback (the IC operates in the overload range). The maximum pulse width is reached at time point  $t_2$  ( $V_2 = V_{2\max}$ ). The IC operates at the overload point. Thereafter the peak values of  $V_2$  decrease rapidly, as the IC is operating within the regulation range. The regulating loop has built up. If voltage  $V_6$  falls below the switch-off threshold  $V_{6\min}$  before the reversal point is reached, the starting attempt is aborted (pin 5 is switched to low). As the IC remains switched on,  $V_6$  further decreases to  $V_6$ . The IC switches off;  $V_6$  can rise again (time point 14) and a new start-up attempt begins at time point  $t_1$ . If the rectified alternating line voltage (primary voltage) collapses during load,  $V_3$  can fall below  $V_{3A}$ , as is happening at time point  $t_3$  (switch-on attempt when voltage is too low). The primary voltage monitor then clamps  $V_3$  to  $V_{3S}$  until the IC switches off ( $V_6 < V_{6A}$ ). Then a new start-up attempt begins at time point  $t_1$ .

### Regulation, Overload and No-Load Behaviour

When the IC has started up, it is operating in the regulation range. The potential at pin 1 typically is 400 mV. If the output is loaded, the regulation amplifier allows broader impulses ( $V_5 = H$ ). The peak voltage value at pin 2 increases up to  $V_{2S \max}$ . If the secondary load is further increased, the overload amplifier begins to regulate the pulse width downward. This point is referred to as the overload point of the power supply. As the IC supply voltage  $V_6$  is directly proportional to the secondary voltage, it goes down in accordance with the overload regulation behaviour. If  $V_6$  falls below the value  $V_{6 \min}$ , the IC goes into burst operation. As the time constant of the half-wave charge-up is relatively large, the short-circuit power remains small. The overload amplifier cuts back to the pulse width  $t_{pk}$ . This pulse width must remain possible, in order to permit the IC to start-up without problems from the virtual short circuit, which every switching on with  $V_1 = 0$  represents. If the secondary side is unloaded, the loading impulses ( $V_5 = H$ ) become shorter. The frequency increases up to the resonance frequency of the system. If the load is further reduced, the secondary voltages and  $V_6$  increase. When  $V_6 = V_{6 \max}$ , the logic is blocked. The IC converts to burst operation. This renders the circuit absolutely safe under no-load conditions.

### Behaviour when Temperature Exceeds Limit

An integrated temperature protection disables the logic when the chip temperature becomes too high. The IC automatically interrogates the temperature and starts as soon as the temperature decreases to permissible values.



## Absolute Maximum Ratings

$T_A = 25\text{ °C}$

Parameter		Symbol	Limit Values		Unit	Remarks
			min.	max.		
Voltages	pin 1	$V_1$	- 0.3	3	V	Supply voltage
	pin 2	$V_2$	- 0.3		V	
	pin 3	$V_3$	- 0.3		V	
	pin 5	$V_5$	- 0.3	$V_6$	V	
	pin 6	$V_6$	- 0.3	20	V	
	pin 7	$V_7$	- 0.3	6	V	
Currents	pin 1	$V_1$		3	mA	$t_p \leq 50\ \mu\text{s}; v \leq 0.1^*$ $t_p \leq 50\ \mu\text{s}; v \leq 0.1$ $t_p \leq 50\ \mu\text{s}; v \leq 0.1$
	pin 2	$V_2$		3	mA	
	pin 3	$V_3$		3	mA	
	pin 4	$V_4$	- 1.5		A	
	pin 5	$V_5$	- 1.5	1.5	A	
	pin 6	$V_6$		1.5	A	
	pin 7	$V_7$		3	mA	
	pin 8	$V_8$	- 3	3	mA	
Junction temperature		$T_j$		125	°C	
Storage temperature		$T_{\text{stg}}$	- 40	125	°C	

## Operating Range

Supply voltage	$V_6$	8	14	V	IC "on"
Ambient temperature	$T_A$	- 20	85	°C	
Heat resistance					
Junction environment	$R_{\text{th JE}}$		100	K/W	measured at pin 4
Junction case	$R_{\text{th JC}}$		70	K/W	

\*)  $t_p$  = pulse width  
v = duty circle

## Characteristics

$T_A = 25\text{ °C}$

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			

### Start-Up Hysteresis

Start-up current	$I_{6E0}$	0.5	1.1	1.6	mA	$V_6 = V_{6E}$	1
Switch-on voltage	$V_{6E}$	11	12	13	V		1
Switch-off voltage	$V_{6A}$	6.4	6.9	7.4	V		1
Switch-on current	$I_{6E1}$	7	9	12	mA	$V_6 = V_{6E}$	1
Switch-off current	$I_{6A1}$	6.5	8	10	mA	$V_6 = V_{6A}$	1

### Voltage Clamp ( $V_6 = 10\text{ V}$ , IC switched off)

At pin 2 ( $V_6 \leq V_{6E}$ )	$V_{2\text{ max}}$	5.6	6.6	7.6	V	$I_2 = 1\text{ mA}$	1
At pin 3 ( $V_6 \leq V_{6E}$ )	$V_{3\text{ max}}$	5.6	6.6	7.6	V	$I_3 = 1\text{ mA}$	1

### Regulation Range

Regulation input voltage	$V_{1R}$	370	400	430	mV		2
Voltage gain regulation range	$-V_R$	47	50	53	dB	$V_R = d(V_{2S} - V_{2B}) / -dV_1$	2
Regulation transmittance	$R_R$		20		k $\Omega$	$R_R = d(V_{2S} - V_{2B}) / -dI_1$	2

### Primary Current Reproducer

Basic value	$V_{2B}$	0.90	1.00	1.15	V		2
Input resistance $R_{2B} = \Delta V_{2B} / \Delta I_{2B}$	$R_{2B}$		25	40	$\Omega$	$V_3 = 1.5\text{ V};$ $1.2\text{ V} < V_2 < 3\text{ V}$ $0.1\text{ mA} < I_{2B} < 3\text{ mA}$	2
Slew rate falling edge	$dV_2/dt$		-1		V		2

## Characteristics (cont'd)

$T_A = 25\text{ °C}$

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			

### Overload Range and Short-Circuit Operation

Overload range lower limit	$V_{1U}$	60	230	290	mV		2
Voltage gain in overload range	$V_{\ddot{U}}$	1	2	3		$V_{\ddot{U}} = d(V_{2S} - V_{2B})/dV_1$	2
Input current in short circuit operation	$-I_1$	90	120	180	$\mu\text{A}$	$V_1 = 0\text{ V}$	2
Peak value in overload range	$V_{2\ddot{U}}$		3.0		V	$V_1 = V_{1R} - 10\text{ mV}$	2
Peak value in short circuit operation	$V_{2K}$	2.2	2.6	3.0	V	$V_1 = 0\text{ V}$	2

### Generally Valid Data ( $V_6 = 10\text{ V}$ )

#### Overload Point Correction

Overload point correction current	$-I_2$	400	660	850	$\mu\text{A}$	$V_3' = 4\text{ V}; V_2' = 0\text{ V}$	1
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#### Zero Transition Detector Voltage

Positive clamp	$V_{8P}$	0.70	0.75	0.80	V	$I_8 = 1\text{ mA}$	2
Negative clamp	$V_{8N}$	-0.15	-0.22	-0.25	V	$I_8 = -1\text{ mA}$	2
Threshold value	$V_{8S}$	40	50		mV		2
Input current	$-I_8$		2	4	$\mu\text{A}$	$V_8 = 0$	2
Delay time between $V_8$ and $V_5$	$t_{d2}$	0.2	0.4	0.7	$\mu\text{s}$		2
Zero detector disable time	$t_{UL}$	2	2	6	$\mu\text{s}$		

**Characteristics (cont'd)**

$T_A = 25\text{ °C}$

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			

**Output Stage**

Saturation voltages S in position 1							
Output sourcing	$V_{Sat0}$		1.5	2.0	V	$I_5 = -0.1\text{ A}$	1
Output sourcing	$V_{Sat0}$		2.5	3.0	V	$I_5 = -1\text{ A}$	1
Output sinking	$V_{SatV}$		1.0	1.2	V	$I_5 = 0.1\text{ A}$	1
Output sinking	$V_{SatV}$		1.4	1.8	V	$I_5 = 0.5\text{ A}$	1
Output slew rate							
Rising slope	$+ dV_5/dt$		50		V/ $\mu$ s		2
Falling slope	$+ dV_5/dt$		80		V/ $\mu$ s		2

**Soft-Start**

Open-circuit	$V_7$	2.2	2.6	2.9	V	$V_1 = 0$	2
Input resistance	$R_{7L}$	4	6	9	k $\Omega$	$0.5\text{ V} \leq V_7 \leq 3\text{ V}$	2
Peak voltage	$V_{2S}$	1.0	1.2	1.4	V	$V_7 = 0$	2

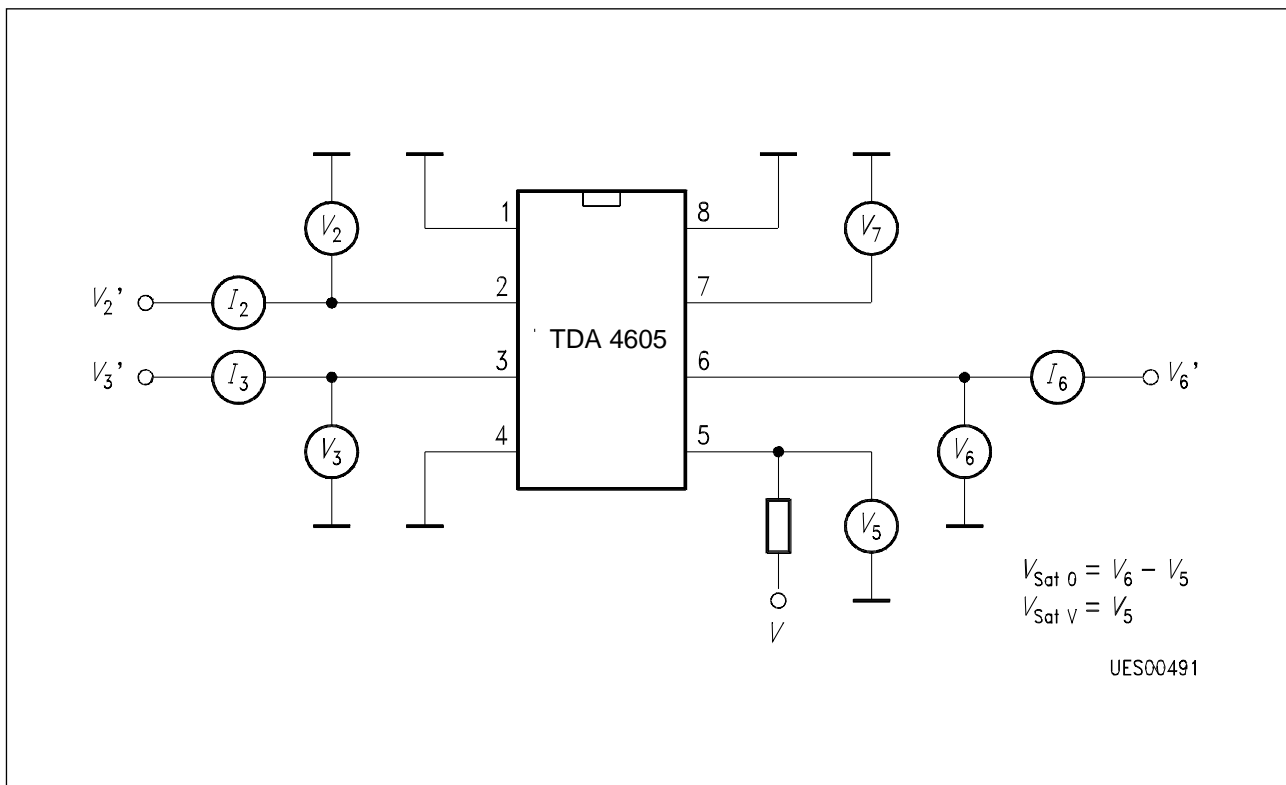
**Protection Circuit**

Undervoltage protection for $V_6$ at pin 5 = $V_{5\text{ min}}$ if $V_6 < V_{6\text{ min}}$ (definition: $V_{6\text{ min}} = V_{6A} + \Delta V_6$ )	$\Delta V_6$		100		mV		2
Overvoltage protection for $V_6$ voltage at pin 5 = $V_{5\text{ min}}$ if $V_6 > V_{6\text{ max}}$	$V_{6\text{ max}}$	14	15	16	V		2
Undervoltage protection for $V_{AC}$ voltage at pin 5 = $V_{5\text{ min}}$ if $V_3 < V_{3A}$	$V_{3A}$	925	1000	1075	mV	$V_{2'} = 0\text{ V}$	1
Over temperature chip temperature for $V_{5\text{ min}}$	$T_j$		125		$^{\circ}\text{C}$	–	2

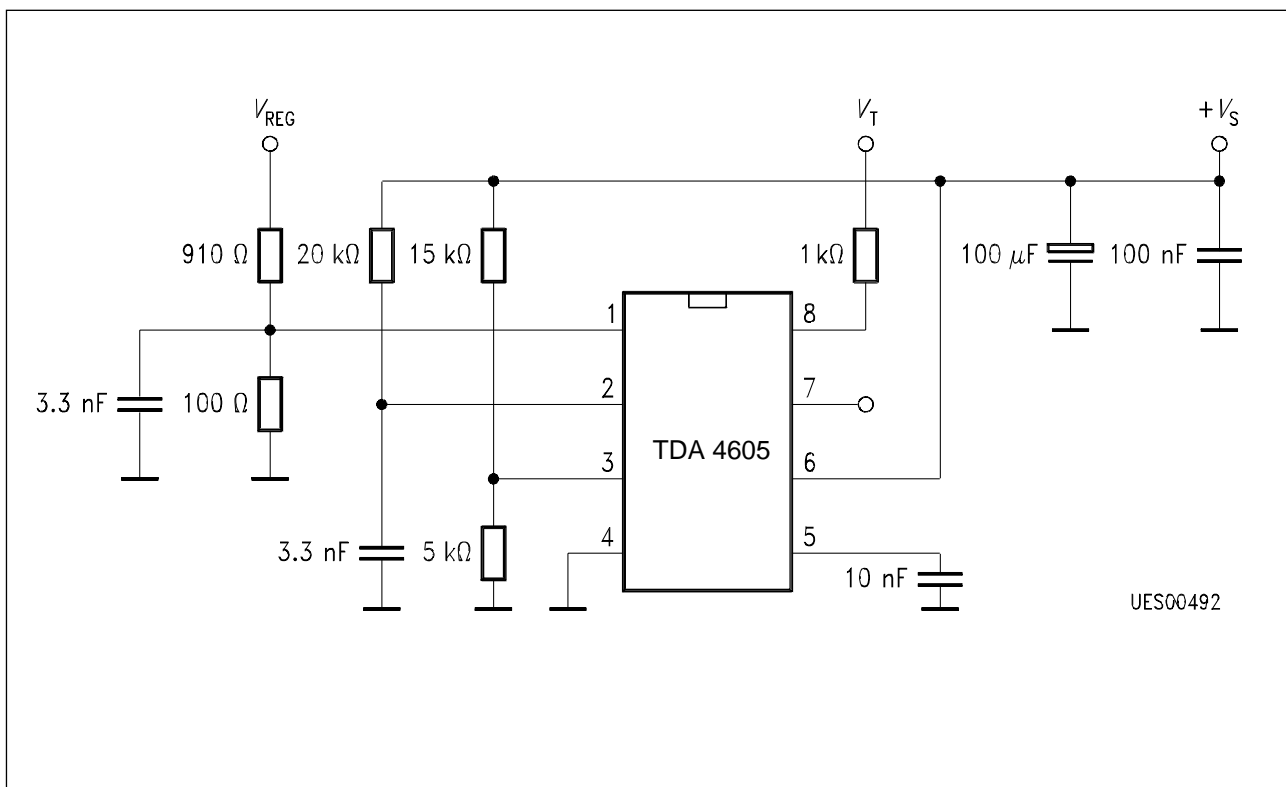
## Characteristics (cont'd)

$T_A = 25\text{ °C}$

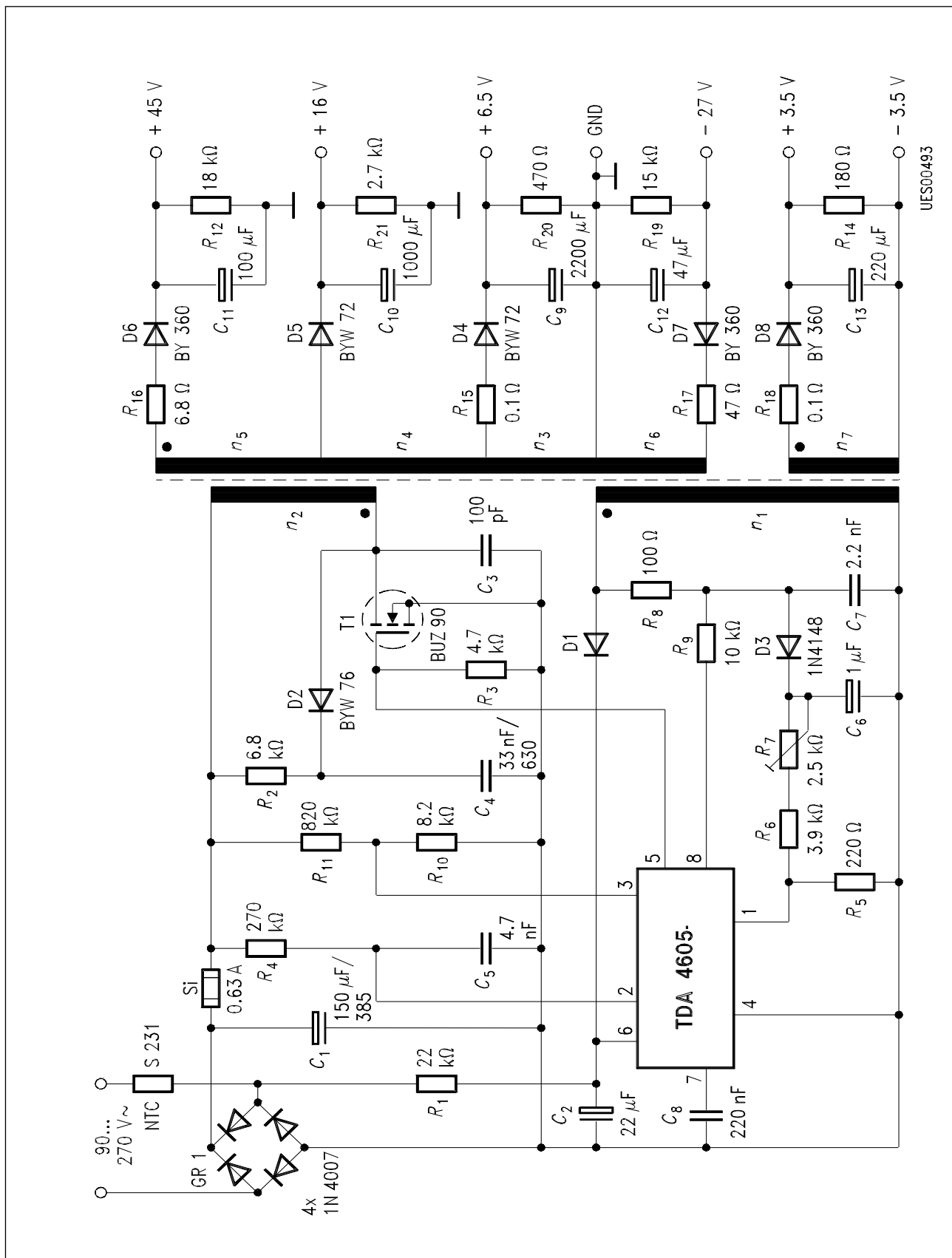
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Voltage at pin 3 when protection function occurred; ( $V_3$ will be clamped until $V_6 < V_{6A}$ )	$V_{3S}$		0.4	0.8	V	$I_3 = 1\text{ mA}$	1
Burst operation quiescent current	$I_6$		8		mA	$V_3 = V_2 = 0\text{ V}$	1



Test Circuit 1



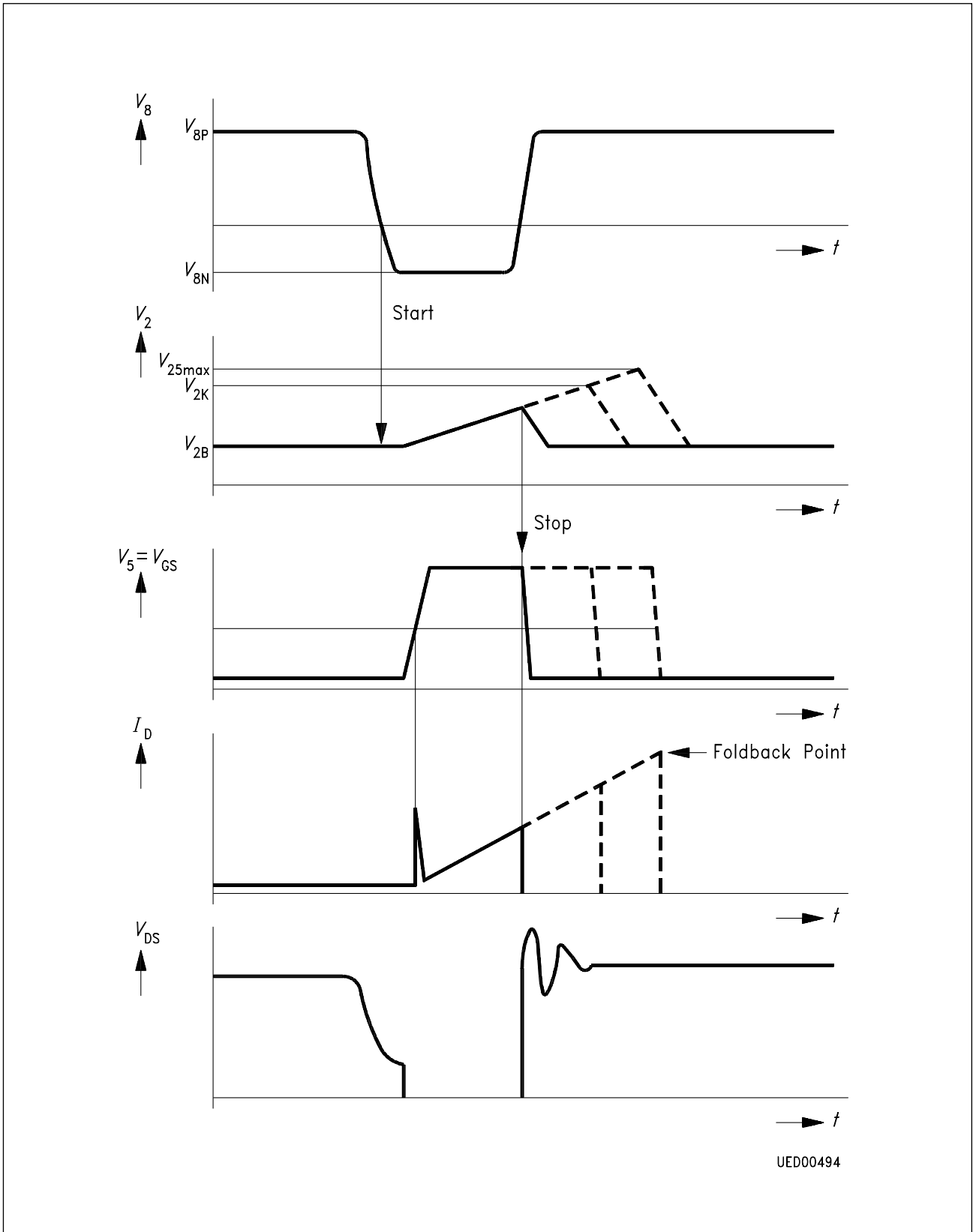
Test Circuit 2



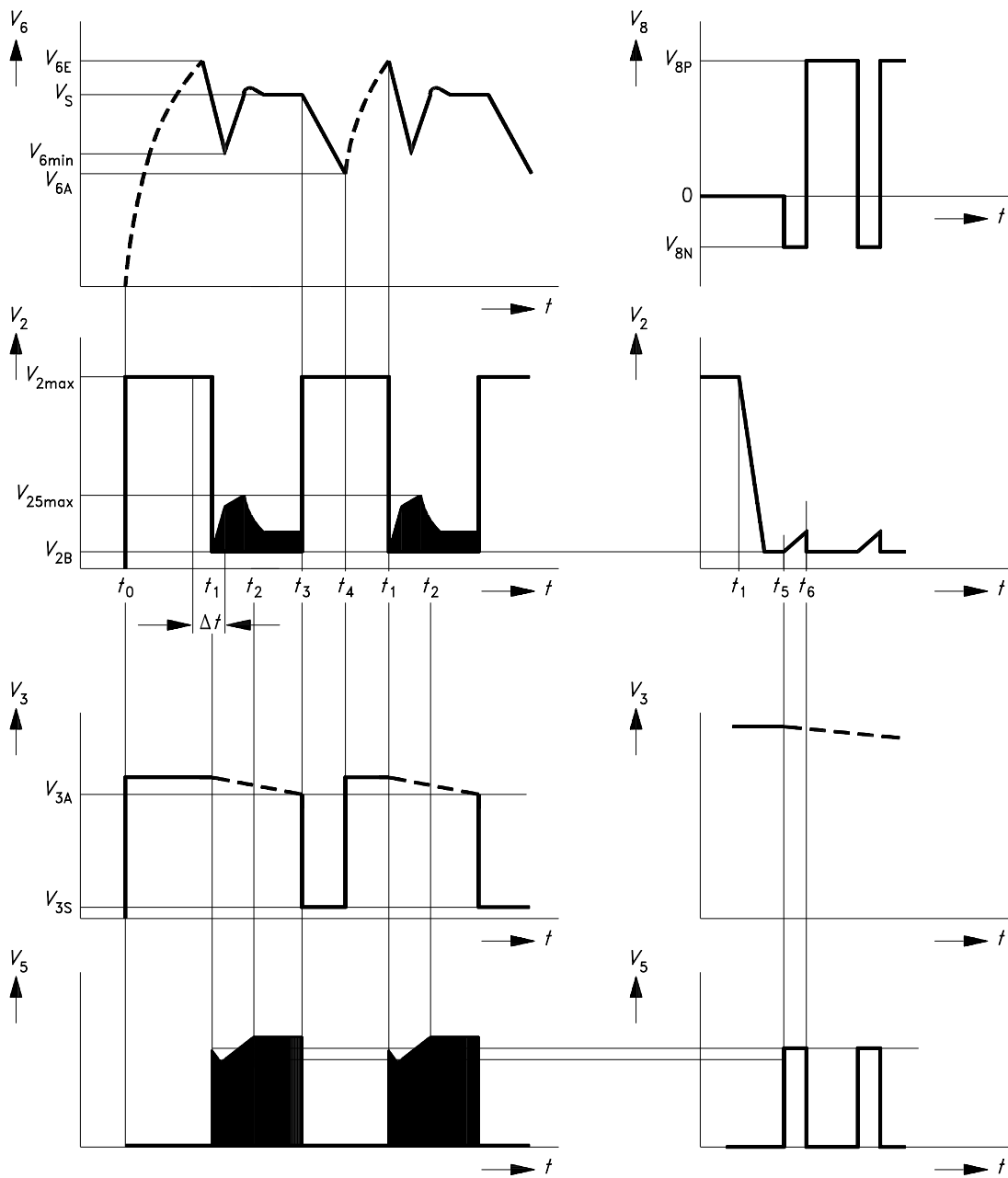
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Application Circuit

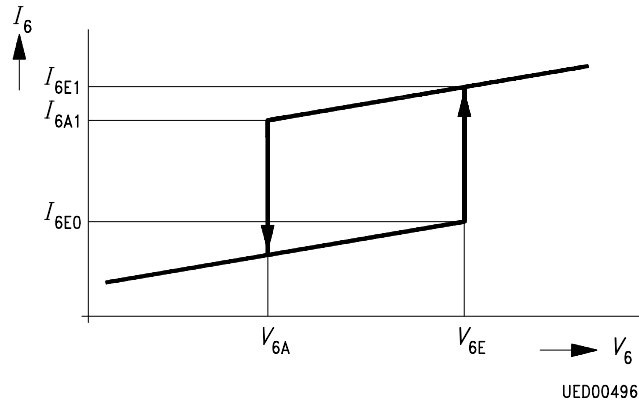
Diagrams



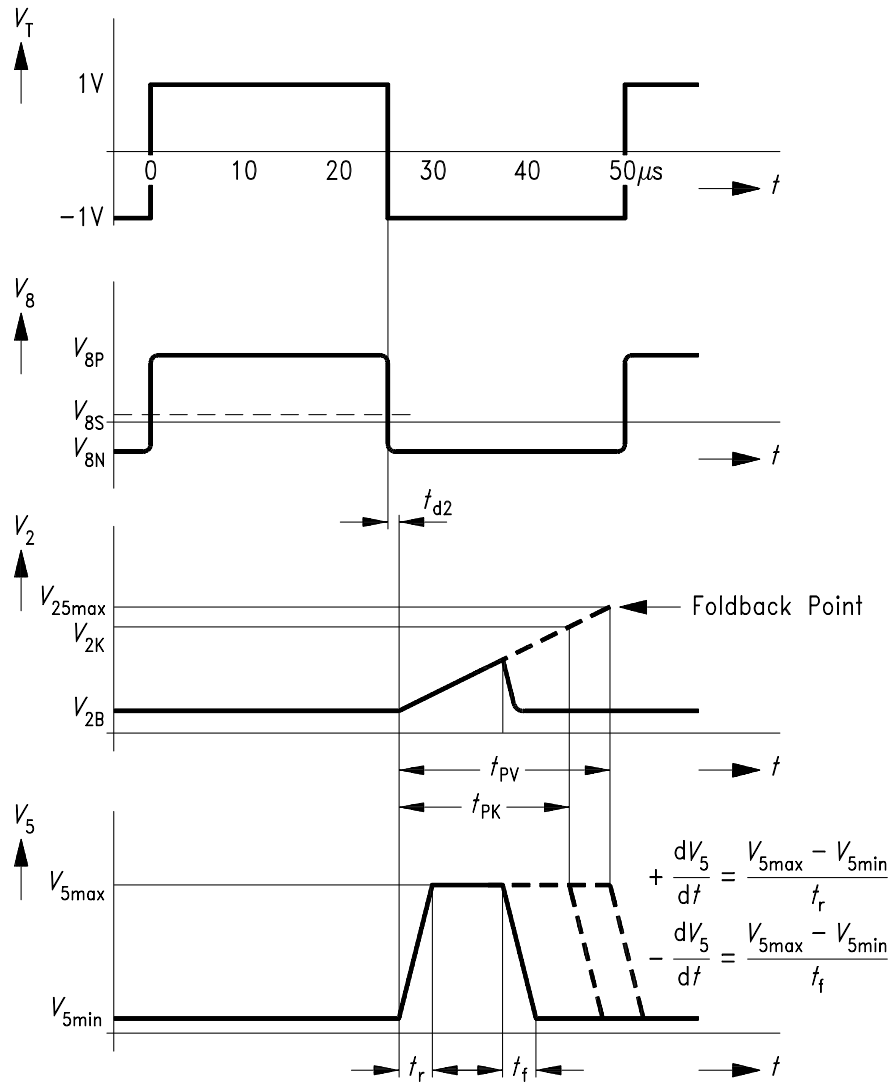




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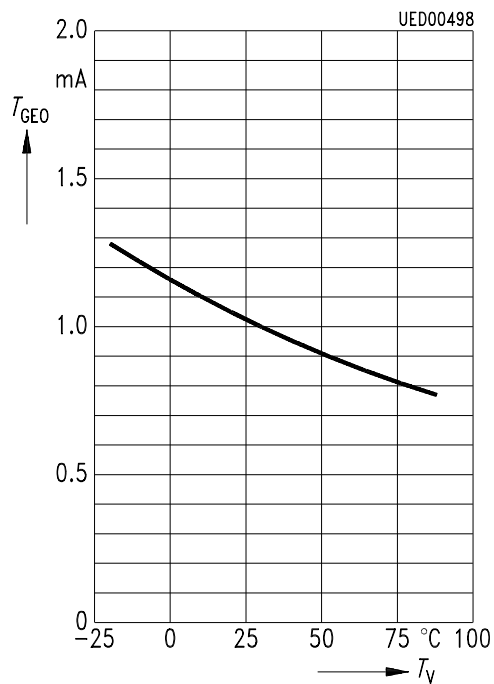
Start-Up Hysteresis



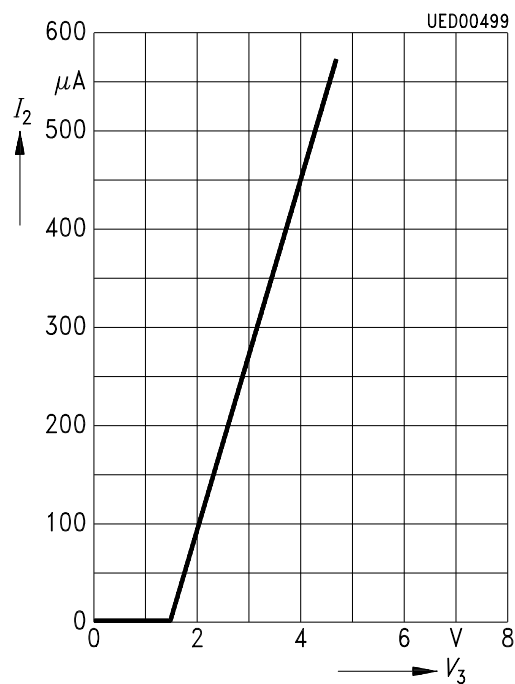
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Operation in Test Circuit 2

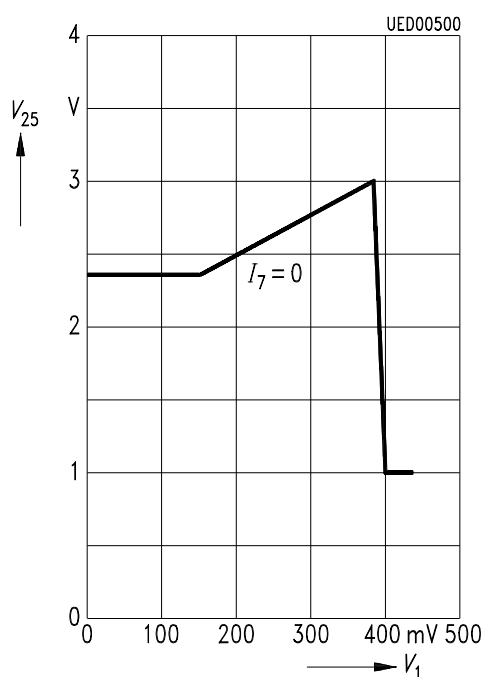
**Start-Up Current as a Function of the Ambient Temperature**



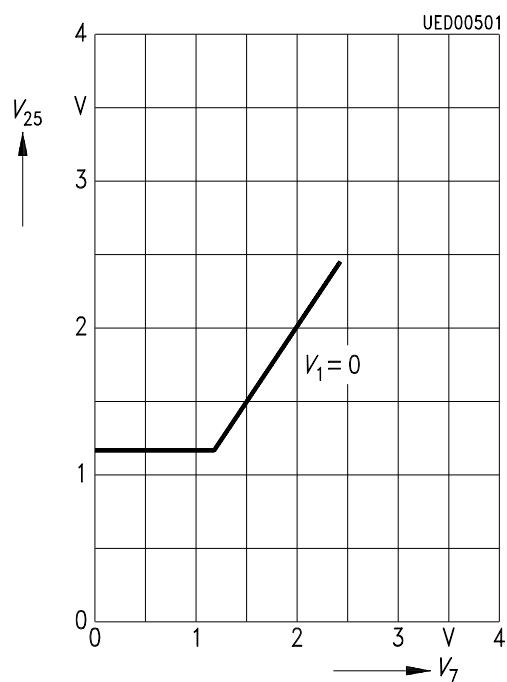
**Overload Point Correction as a Function of the Voltage at Pin 3**



**Peak Value of the Primary Current Reproduction Voltage as a Function of the Regulating Voltage**

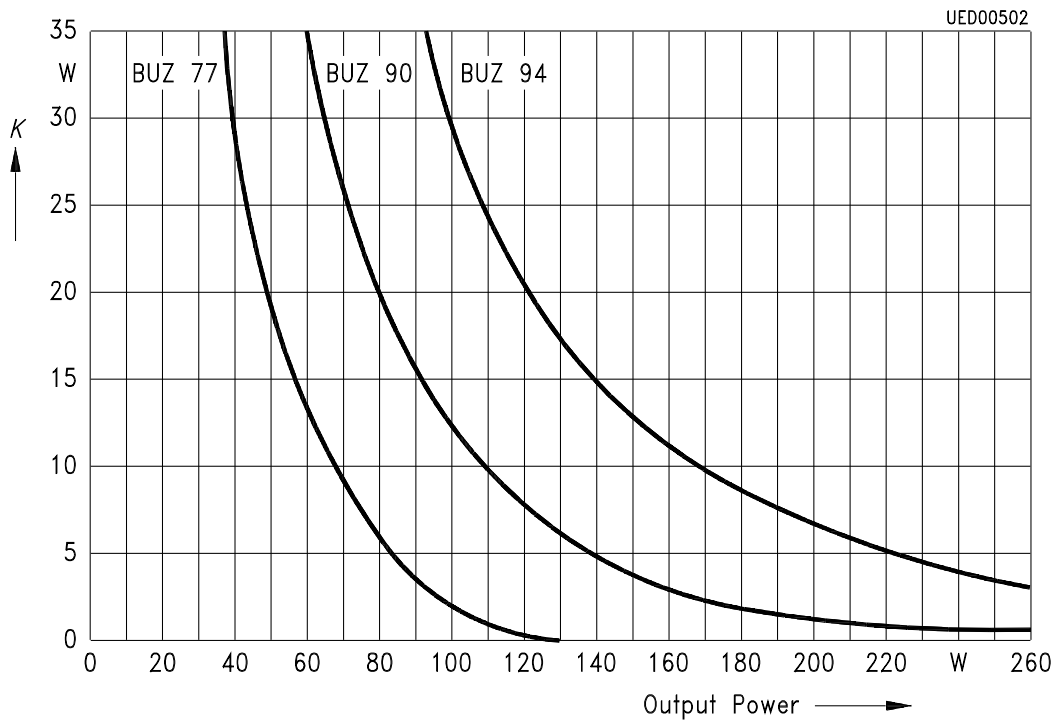


**Peak Value of the Primary Current Reproduction Voltage by Loading Pin 7**



## Recommended Heat Sink by 60 °C Ambient Temperature

Narrow Range 180 V ... 270 V ~



Narrow Range 180 V ... 270 V ~

