Power Transistors Fabricated Using Isotopically Purified Silicon (^{28}Si)

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***Abstract*—It is well known that isotopic purification of group IV elements can lead to substantial increases in thermal conductivity due to reduced scattering of the phonons. The magnitude of the increase in thermal conductivity depends on the level of isotopic purification, the chemical purity, as well as the test temperature. For isotopically pure silicon (^{28}Si) thermal conductivity improvements as high as sixfold at 20 K and 10%–60% at room temperature have been reported. Device heating during operation results in degradation of performance and reliability (electromigration, gate oxide wearout, thermal runaway). In this letter, we discuss the thermal performance of packaged RF LDMOS power transistors fabricated using ^{28}Si. A novel technique allows the cost effective deployment of this material in integrated circuit manufacturing. A clear reduction of about 5 °C–7 °C in transistor average temperature and a corresponding 5%–10% decrease in overall packaged device thermal resistance is consistently measured by infrared microscopy in devices fabricated using ^{28}Si over natural silicon.**

***Index Terms*—Heat extraction, isotopically pure silicon (^{28}Si), power dissipation, reliability, RF LDMOS transistor, thermal design.**

I. Introduction

DEVICE heating during transistor operation results in degradation of performance, reliability (electromigration, gate oxide wearout, thermal runaway), and represents one of the major challenges facing integrated circuit design. Various heat extraction strategies have been proposed to mitigate this issue [1]. In this letter, we attempt a materials solution to this problem and discuss the thermal performance of packaged RF LDMOS power transistors fabricated using isotopically purified silicon (^{28}Si). A layer transfer technique allowed the cost effective deployment of this material in integrated circuit manufacturing for the first time.

Temperature gradients result in a proportional thermal current density. The proportionality constant in this description of heat flow is defined as the thermal conductivity. Thermal conductivity of a solid is ultimately limited by phonon scattering and determined by crystal structure, temperature, purity, and geometry. In the case of high quality samples (where most imperfections have been removed) three regimes of temperature dependence are observed. First, the T^3 increase at low temperatures caused by sample boundary scattering. Second, the T^{-1} dependent decrease at high temperatures due to *Umklapp* resistance (crystal momenta in phonon collisions is conserved within a nonzero reciprocal lattice vector). In between these limits, a thermal conductivity maximum (in the mathematical form of $T^n e^{b/T}$) emerges [2]. The peak value of thermal conductivity is limited by the level of purity of the sample. In integrated circuit grade natural silicon the largest concentration of defects that would affect the thermal conductivity are the other isotopes of silicon. Natural silicon is composed of three stable isotopes: 92% ^{28}Si, 4.7% ^{29}Si, and 3.3% ^{30}Si. The density (concentration) of imperfections in the form of isotopes (8%) far exceed any other defects (e.g., doping) and is the dominant scattering mechanism for the phonons that transport heat. It has been shown experimentally and theoretically that isotopic purification of group IV elements (^{12}C, ^{28}Si, ^{74}Ge) leads to significant increases in thermal conductivity [2]–[12]. In the case of isotopically pure silicon (99.9% ^{28}Si) a peak thermal conductivity of 30 000 W/m-K is measured at 20 K. This represents an improvement of sixfold over natural silicon. However there is significant scatter in the data for the extent of the improvement (10% to 60%) in the 300 K–400 K range [3]–[7]. For "undoped" silicon at room temperature the range of measured thermal conductivity is: 142–148 W/m-K (natural Si) versus 165–227 W/m-K (^{28}Si). Thermal conductivity degrades with increased doping by about 20% for both natural Si and ^{28}Si for an acceptor concentration of 2×10^{19} cm^{-3} [6]. The purpose of this letter is twofold. First, to assess the thermal properties of a power semiconductor device fabricated using ^{28}Si. Second, to document a layer transfer technique that allows the cost effective deployment of ^{28}Si.

II. Process Integration and Device Fabrication

We have chosen RF LDMOS (laterally diffused) power transistors that are used in base stations as the demonstration vehicle since heat extraction and the reduction of the operating junction temperature is a major consideration. Device heating during operation will result in degradation of performance (mobility) and reliability. Most of the major failure mechanisms in semiconductor devices such as electromigration, gate oxide wearout, and thermal runaway are all accelerated by increased temperature. Transistor mean time to failure decreases by a factor of two for every 9 °C increase in junction temperature (corresponding to an activation energy of ~1.0 eV) for our device. RF LDMOS transistor is a three-terminal discreet device with gate and drain contact on top and the device source region is shunted to the underlying heavily doped p$^+$ substrate via a plug or sinker [13]–[17]. After being fully processed the wafers are thinned to 50 μm for heat extraction. Subsequently, the backside of the wafer forms the source contact. Hence, our strategy utilizes epitaxial deposition of ^{28}Si in combination with a wafer thinning

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technique to fabricate cost effective [18] integrated circuits with improved thermal performance. The starting material is natural silicon p^+ type (100) wafers. On this substrate, a dual layer of 99.9% ^{28}Si is epitaxially deposited using trichlorosilane which was chemically converted from isotopically purified silicon tetraflouride. The layer structure is composed of about 40 μm of heavily doped (2×10^{19} cm^{-3} boron) p^+-^{28}Si followed by about 8 μm of undoped (resistivity$>$ 100 $\Omega \cdot$ cm) ^{28}Si. Natural silicon wafers (8 μm epi) were also included in the lot as a control. Standard wafer processing follows. The RF LDMOS device fabricated for this study has a gate length of 0.65 μm and a lightly doped drift region of 3.0 μm. Gate oxide thickness is 350 Å. The breakdown voltage of the transistor is 75 V. The device nominally operates at $V_{\rm DS} = 28$ V [17]. After standard wafer processing the backside natural silicon substrate is removed by grinding. The final silicon die thickness is 50 ± 3 μm and is composed almost entirely of ^{28}Si (except control devices). Since the self-diffusion coefficient of silicon is $\sim 5 \times 10^{-15}$ cm^2/s at 1100 °C [19] the final up-diffusion from the natural Si substrate into ^{28}Si layer is much less than 0.5 μm. As expected wafer level measurements indicate no differences in electron transport and hot electron aging.

III. Infrared Thermal Measurements

Infrared measurements of the operating junction temperature were performed using a state-of-the-art Quantum Focus Instruments Infrascope II. For these measurements, 17 devices fabricated on natural as well as ^{28}Si substrates were assembled on identical packages, by means of AuSi eutectic die attach. Both standard Kyocera Cu–W and Cu-flanged packages were utilized. The devices were mounted on a RF fixture, matched and terminated to avoid oscillations. A thermocouple mounted immediately next to the package allowed for a precise determination of the case temperature. Transistors with 80 mm (45 W rated) and 120 mm (60 W rated) device width are evaluated. The silicon die is about 1.5 by 5.5 mm. The 120-mm width test transistor is designed to reduce the dissipated power density by spreading the active area. Fig. 1 shows the infrared image (contour map) for the 80-mm ^{28}Si and natural Si devices in a Cu–W package dissipating 50 W (0.65 W/mm). Fig. 2 shows the infrared image comparison for 120-mm devices in a Cu package dissipating 80 W (0.75 W/mm). The case temperature is maintained around $\sim$ 70 °C. The images show the expected profile in junction temperature, where due to boundary conditions the center of the die is the hotter region (125 °C–140 °C). Devices fabricated on a ^{28}Si substrate run on average 5 °C–7 °C cooler corresponding to a non-negligible 1.5 times improvement in extrapolated lifetime. To facilitate a more direct comparison the temperature profile along a line that runs longitudinally in the middle of the die is presented in Fig. 3(a) and (b). Thermal resistance (°C/W) of the packaged transistor structures (die, die attach, package) can be calculated by dividing the increase in average temperature above the case temperature by the power dissipated (Figs. 1 and 2). A 5%–10% reduction in overall thermal resistance is consistently measured in all of the structures we have fabricated that use ^{28}Si. While we know that the main contributors to the junction-to-case thermal resistance are heat conduction through the Si die and the package

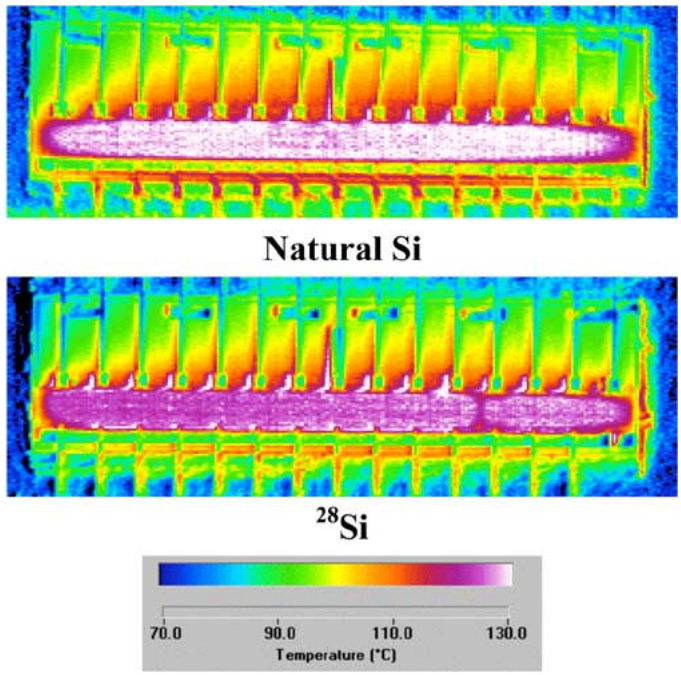

Fig. 1. IR imaged thermal contour maps (top view) compare the thermal performance of 80-mm devices in Cu–W package fabricated using natural Si (top) versus isotopically pure ^{28}Si (bottom). Natural silicon (top) average case temperature $T_c = 72$ °C, junction temperature $T_j = 129$ °C, power dissipation $P_{\rm diss} = 50.4$ W, and thermal resistance is $\Theta = 1.13$°C/W. For ^{28}Si (bottom) device $T_c = 72$ °C, $T_{\rm j} = 124$ °C, $P_{\rm diss} = 51.0$ W, and $\Theta = 1.02$ °C/W.

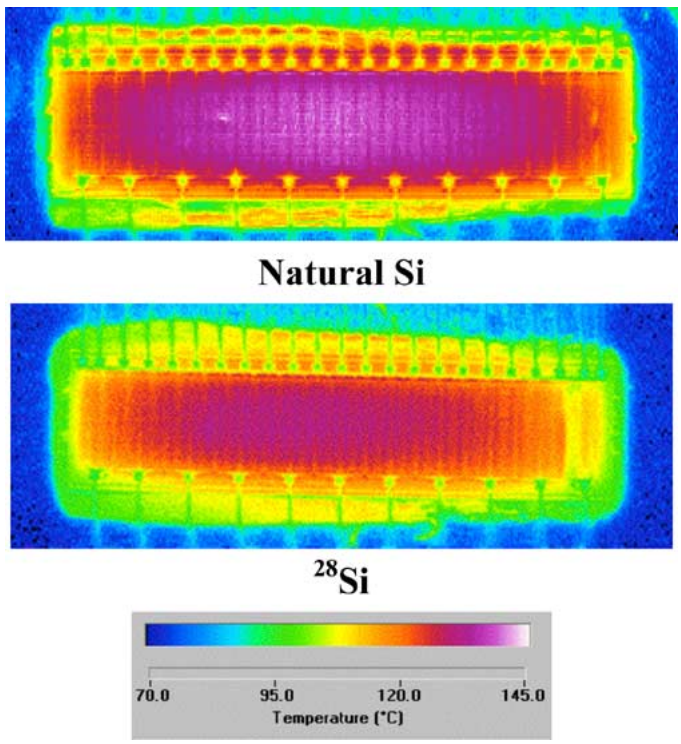

Fig. 2. IR imaged thermal contour maps compare the thermal performance of 120 mm devices in Cu package fabricated using natural Si versus isotopically pure ^{28}Si. Natural silicon (top) $T_c = 74$ °C, $T_j = 136$ °C, $P_{\rm diss} = 80$ W, and $\Theta = 0.78$ °C/W. For ^{28}Si (bottom) device $T_c = 74$ °C, $T_j = 129$ °C, $P_{\rm diss} = 80.0$ W, and $T = 0.70$ °C/W.

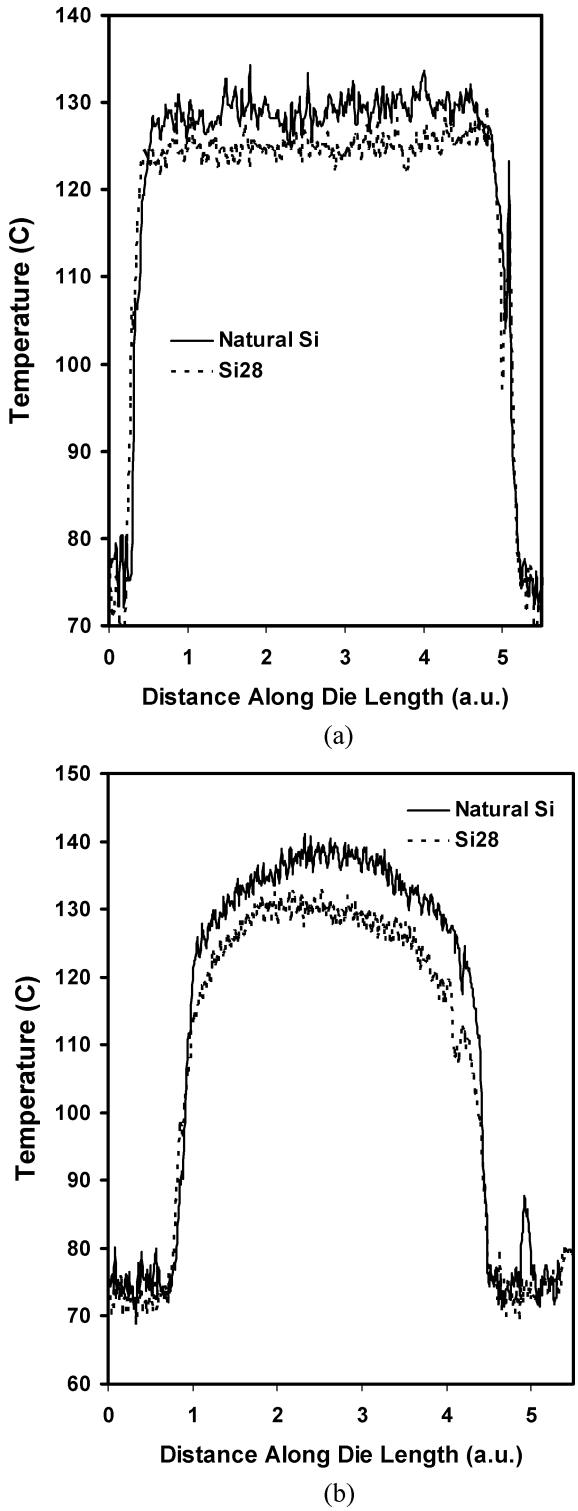

Fig. 3. Temperature profile generated from the IR image given in Figs. 1 and 2 comparing the thermal performance of transistors fabricated using natural Si versus isotopically pure ^{28}Si. (a) 80-mm total width transistor in Cu–W package and (b) 120-mm total width transistor in Cu package.

(Cu–W or Cu) our experiment is too convoluted and device structure sufficiently complicated for self-consistently extracting the exact value of thermal conductivity coefficients for natural and isotopically pure silicon.

IV. Conclusion

In summary, a novel layer transfer technique deploying isotopically pure ^{28}Si was discussed. RF LDMOS transistors were fabricated using this methodology. A clear reduction of about 5 °C–7 °C in transistor average temperature is measured by infrared microscopy as compared with devices fabricated using natural Si. The transistors otherwise are electrically identical. The use of ^{28}Si may complement other strategies for heat extraction from integrated circuits.

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References

[1] P. E. Ross, "Beat the heat," *IEEE Spectrum*, no. 5, pp. 38–43, May 2004.
[2] J. M. Ziman, *Electrons and Phonons*. Oxford: Clarendon, 1960.
[3] T. Ruf, R. Henn, M. Asen-Palmer, E. Gmelin, M. Cardona, H. Pohl, G. Devyatych, and P. Sennikov, "Thermal conductivity of isotopically enriched silicon," *Solid State Commun.*, vol. 115, pp. 243–247, 2000.
[4] D. G. Cahill and F. Watanabe, "Thermal conductivity of isotopically pure and Ge doped Si epitaxial layers from 300 to 550 K," *Phys. Rev. B, Condens. Matter*, vol. 70, pp. 2 353 221–2 353 223, 2004.
[5] T. Ruf, R. Henn, M. Asen-Palmer, E. Gmelin, M. Cardona, H. Pohl, G. Devyatych, and P. Sennikov, *Erratum to "Thermal Conductivity of Isotopically Enriched Silicon"*, vol. 127, p. 257, 2003.
[6] P. L. Komarov, M. Burzo, G. Kaytaz, and P. Raad, "Transient thermo-reflectance measurements of the thermal conductivity and interface resistance of metallized natural and isotopically pure silicon," *Microelectron. J.*, vol. 34, pp. 1115–1118, 2003.
[7] W. S. Capinski and H. J. Maris, "Thermal conductivity of isotopically enriched silicon," *Appl. Phys. Lett.*, vol. 71, pp. 2109–2111, 1997.
[8] G. A. Slack, "Effect of isotopes on low-temperature thermal conductivity," *Phys. Rev.*, vol. 105, pp. 827–831, 1957.
[9] T. H. Geballe and G. W. Hull, "Isotopic and other types of thermal resistance in germanium," *Phys. Rev.*, vol. 110, pp. 773–775, 1958.
[10] T. R. Anthony, W. Banholzer, J. Fleischer, L. Wei, P. Thomas, and R. Pryor, "Thermal diffusivity of isotopically enriched ^{12}C diamond," *Phys. Rev. B, Condens. Matter*, vol. 42, pp. 1104–1111, 1990.
[11] J. Graebner, T. Hartnett, and R. Miller, "Improved thermal conductivity in isotopically enriched chemical vapor deposited diamond," *Appl. Phys. Lett.*, vol. 64, pp. 2549–2551, 1994.
[12] V. I. Ozhogin, A. Inyushin, A. Taldenkov, A. Tikhomirov, G. Popov, E. Haller, and K. Itoh, "Isotope effect in the thermal conductivity of germanium single crystals," *JETP Lett.*, vol. 63, pp. 490–494, 1996.
[13] A. Wood, C. Dragon, and W. Burger, "High performance silicon LDMOS technology for 2 GHz RF power amplifier applications," in *IEDM Tech. Dig.*, 1996, pp. 87–90.
[14] J. G. Fiorenza and J. L. del Alamo, "Experimental comparison of RF power LDMOSFETs on thin film SOI and bulk silicon," *IEEE Trans. Electron Devices*, vol. 49, no. 5, pp. 687–692, May 2002.
[15] H. Brech, W. Brakesiek, D. Burdeaux, W. Burger, C. Dragon, G. Formicone, B. Pryor, and D. Rice, "Record efficiency and gain at 2.1 GHz of high power RF transistors for cellular and 3G base stations," in *IEDM Tech. Dig.*, 2003, pp. 359–362.
[16] L. Vestling, J. Ankarcrona, and J. Olsson, "Analysis and design of a low-voltage high-frequency LDMOS transistor," *IEEE Trans. Electron Devices*, vol. 49, no. 11, pp. 976–980, Nov. 2002.
[17] S. Xu, F. Baiocchi, H. Safar, J. Lott, A. Shibib, Z. Xie, T. Nigam, B. Jones, B. Thompson, J. Desko, and P. Gammel, "High power silicon RF LDMOSFET technology for 2.1 GHz power amplifier applications," in *ISPSD Tech. Dig.*, 2003, pp. 190–193.
[18] S. Burden, "High thermal conductivity silicon," in *Semiconductor FabTech.*, 13th ed. London: ICG, 2001, pp. 297–300.
[19] *Quick Reference Manual*, Wiley, New York, 1984.