High Thermal Conductivity Silicon

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Abstract

Isotopically purified silicon has been verified to have substantially higher thermal conductivity than natural silicon. The benefits of this ultra-purified silicon are discussed and initial device data presented. The cost and availability of epitaxial, SOI and bulk wafers are discussed.

BACKGROUND

An increase in the thermal conductivity of isotopically purified semiconductors was first demonstrated by Geballe and Hull of Bell Labs using germanium-74 in 1958 [1]. This discovery did not generate much interest outside of the physics community until researchers at General Electric and Wayne State University discovered that isotopically purified carbon-12 diamond exhibited a 50% increase in thermal conductivity at room temperature [2]. Further work on germanium and diamond confirmed this effect and extended the measurements to low temperatures, where the thermal conductivity of 99.9% carbon-12 diamond was found to be at least five times higher than that of natural diamond [3–6]. In 1999, researchers at the Max Planck Institute and Brown University found a similar effect in silicon thin films [7], and this work was confirmed with small-diameter bulk silicon crystals in 2000 [8].

Natural silicon contains three stable isotopes, ^{28}Si (92.0%), ^{29}Si (4.7%) and ^{30}Si (3.3%). An otherwise perfect crystal of silicon will contain imperfections in the form of isotopes of different mass, with the density of these imperfections amounting to nearly 8% (Table 1). This far exceeds the doping levels and density of imperfections ordinarily found in semiconductor-quality crystals.

In semiconductor materials, unlike metals, electrons are responsible for the electrical conductivity, while lattice vibrations (phonons) are the mechanism for thermal conductivity. Because the minority isotopes have been removed, silicon-28 crystals have a more perfect crystal lattice, which minimises phonon scattering and leads to higher thermal conductivity without affecting the electrical conductivity.

Figure 1 shows the thermal conductivity of 99.85% isotopically pure silicon-28 as a function of temperature as measured by Ruf et al. [8]. The conductivity is 60% greater than that of natural silicon at room temperature and 600% higher at 20 K. These measurements were performed using steady-state thermal analysis with small-diameter single crystals.

Table 1.
Typical impurities in semiconductor grade silicon

Impurity type	Concentration (atoms per cm3)
Dopant atoms	10^{15} to 10^{20}
Heavy metals	10^{10} to 10^{11}
Oxygen	10^{17} to 10^{18}
^{29}Si and ^{30}Si	4×10^{21}

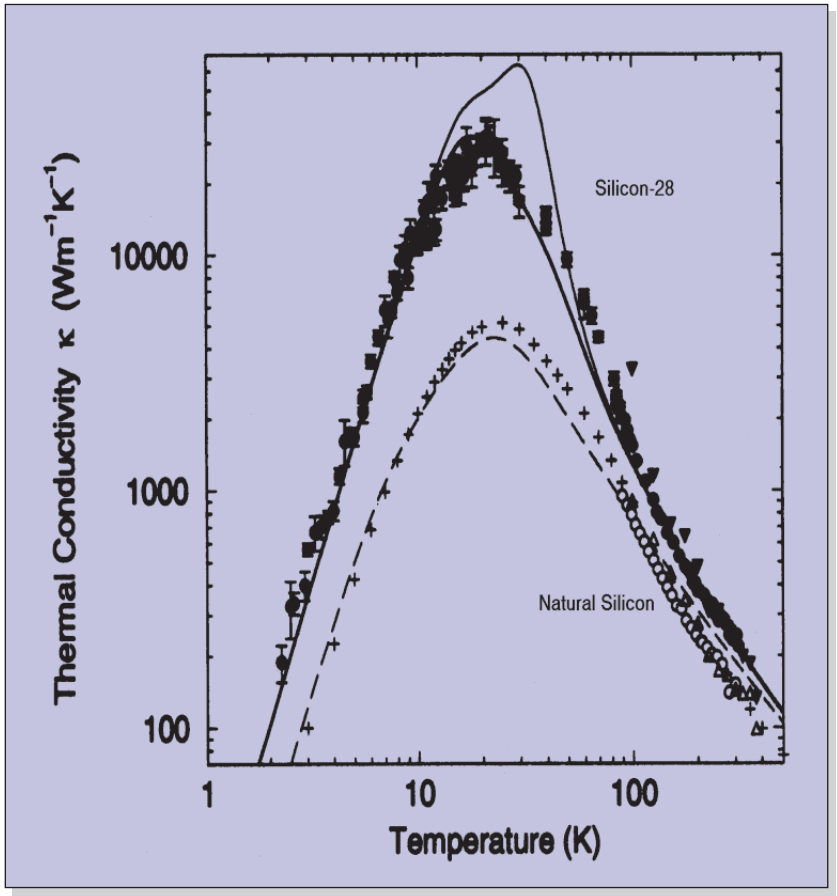


Figure 1
Thermal conductivity of silicon, after Ruf et al. [8]

ADVANTAGES OF ISOTOPICALLY PURE SILICON

Improvement in the thermal conductivity of silicon is important because as transistor size decreases, the current density increases, and more heat is generated per unit volume, causing device operating temperatures to rise. The semiconductor industry is moving towards lower operating voltages and sophisticated mechanical systems to minimise this heat build-up, but greater heat dissipation on the microscale is becoming essential to improve device performance and reliability. The range of potential benefits to device manufacturers from the use of isotopically pure silicon includes manufacturing, performance and design benefits.

Manufacturing Benefits

Normal manufacturing processes produce variations in transistors owing to variations in drain/source size, wafer flatness, dopant implants, contact resistance, etc. These variations produce current density variations and local "hot spots" in the integrated circuit. These hot spots can reduce the device performance since the electron mobility decreases with increasing temperature, and junction leakage increases. This is one reason that microprocessors are speed-sorted after final manufacturing. From the same processed wafer, some microprocessors will run reliably at 1000 megahertz, for example, but some will only run at 800 megahertz or below, reducing yields and revenue to the company. The problem gets worse as the switching speed increases, since power dissipation increases with increasing frequency. Isotopically pure silicon-28 can minimise the effect of these "hot spots" by providing localised heat spreading, producing a larger number of higher-speed chips and more usable chips per wafer.

Another aspect is the manufacturing process itself. Several hundred process steps are required to manufacture a complex integrated circuit and many of them require high temperatures. The uniformity of devices depends on holding the process temperature uniform across the entire wafer. This is becoming more difficult as manufacturers move to 300 mm diameter wafers and rapid thermal processing (RTP). Holding processing temperatures to within ±1°C across the wafer is a major challenge to equipment manufacturers. A higher-thermal-conductivity silicon wafer will make this easier to achieve.

TABLE 2.
COMPARATIVE COOLING COSTS

Cooling technique	Cost per microprocessor
Cryogenic cooler	$350 and up
Thermoelectric cooler	$35
Heat pipes	$10 to $20
Fan and heat sink	$5 to $10
Chip thinning	$1 to $2
Si-28 epi wafers	$0.10 to $1.0*
Si-28 bulk wafers	$1 to $10*

* Incremental to natural silicon wafers

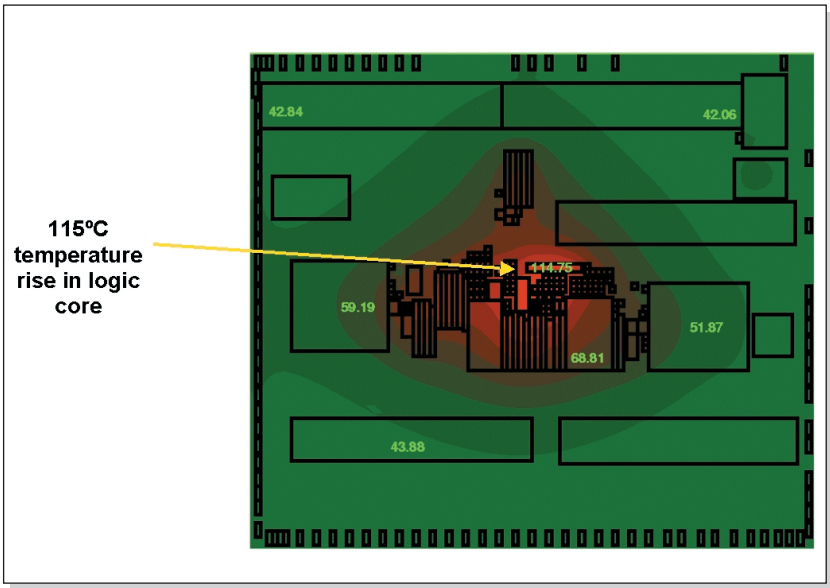


Figure 2
Peak temperature distribution in an experimental IBM microprocessor [10]. Numbers refer to peak temperature rise above ambient

Performance Benefits

Most of the heat generated in a microprocessor occurs in the logic core, where 5 to 10 million transistors are operating at full rated speed. This area comprises only about 5–10% of the area of the silicon chip, and localised temperatures can exceed 150°C. Getting the heat out of this small area and into the remainder of the chip and the package is an engineering challenge that silicon-28 can effectively address. Lower transistor junction temperatures due to isotopically pure silicon-28 will directly improve transistor performance owing to higher carrier mobilities, reduced junction leakage in logic devices, reduced charge leakage in memory devices and reduced metal electromigration. The lower temperatures possible will improve the reliability and lifetime of critical devices. It has been estimated by Intel [9] that a 10°C temperature decrease can double the lifetime of a device.

The results of thermal modelling of an experimental microprocessor design using a normal 200 mm diameter silicon wafer are shown in Figure 2. The peak temperature rise in the logic core is estimated to be about 115°C above ambient. On the basis of this model, the use of a bulk silicon-28 wafer with 60% higher thermal conductivity would decrease the peak temperature by up to 35°C. This would not only significantly increase the performance of this device, but also minimise the cooling requirements for reliable operation.

Design Benefits

The higher thermal conductivity of isotopically pure silicon will allow higher-density circuits to be designed with smaller die sizes and more chips per wafer, resulting in reduced costs. Isotopically pure silicon can be combined with other advanced wafer technologies such as silicon-on-insulator (SOI) and silicon-on-sapphire (SOS) wafers, where thermal management is of critical interest owing to the electrical and thermal insulation of the active silicon layer. For example, silicon–germanium heterojunction bipolar transistors (HBTs) are being developed for high-frequency devices in telecommunication applications. Although Si–Ge transistors have higher carrier mobilities than silicon, the thermal conductivity of Si–Ge alloys is substantially less than that of pure silicon, leading to higher junction temperatures.

TABLE 3.
SILICON ISOTOPE SEPARATION METHODS

Technology	Status	Locations
Gas centrifuge	Production	US, Russia, Europe
Chemical exchange	Production	US, Russia
Lasers	R&D	US, Russia, Japan, Australia

Other, more subtle benefits may also be available with isotopically pure silicon. As device dimensions shrink, the gate oxide thickness in CMOS devices also must decrease. As the transistor size approaches 0.1 micron, the gate oxide thickness will be about 2 nanometres (0.002 microns) or less. This is equivalent to four or five atomic layers of silicon dioxide. The gate oxide integrity (GOI) or breakdown voltage of oxides of this thickness is a key stumbling block to making smaller devices. The more perfect crystal structure of isotopically pure silicon and silicon dioxide may lead to improved gate oxide integrity and fewer carrier surface traps at the silicon–silicon dioxide interface. It has already been shown that the use of deuterium, an isotope of hydrogen, instead of normal hydrogen during the processing of CMOS devices has led to reduced "hot electron" damage and 50 to 100 times longer lifetimes before oxide wear-out [11].

Even though silicon-28 wafers will cost somewhat more than natural-silicon wafers, semiconductor manufacturers will obtain a net cost saving by their use, through higher yields and reduced costs for external cooling systems. Silicon-28 is not only very cost-competitive with alternative cooling solutions for advanced microprocessors (Table 2), but is also synergistic with these techniques to produce the maximum benefit. Most importantly, these advantages are available without any changes in current equipment or process technology. Wafers made from isotopically purified silicon-28 are a one-for-one substitution for normal silicon wafers.

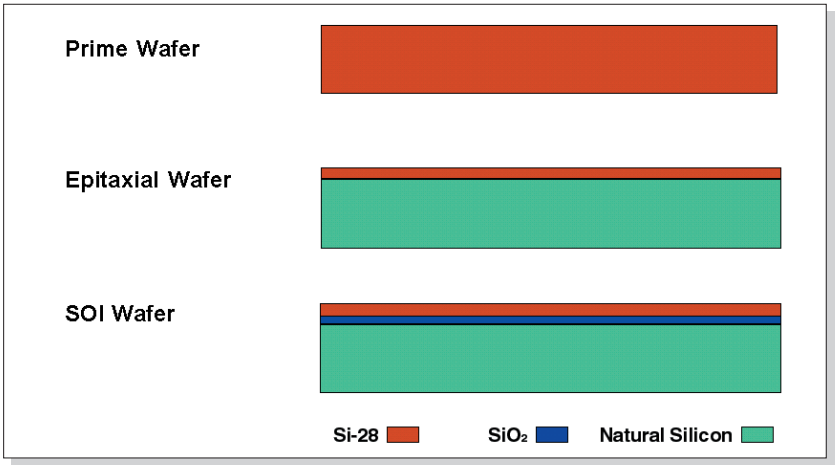
ISOTOPE MANUFACTURING

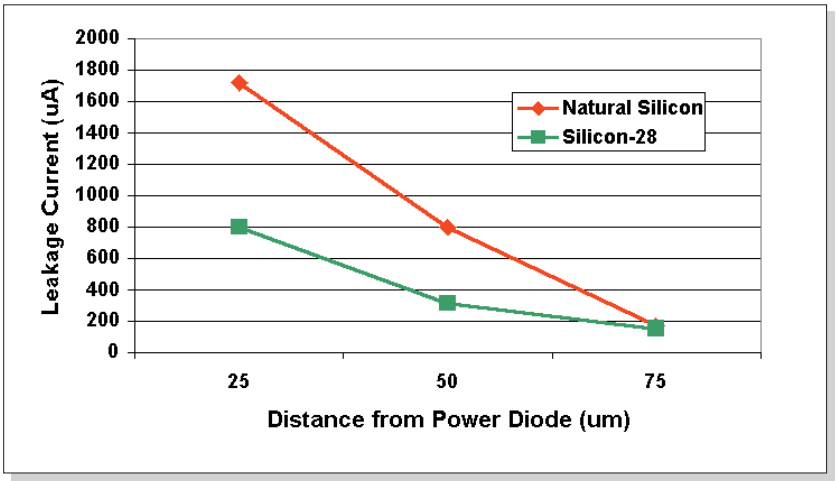
A variety of isotope separation methods have been developed throughout the world (Table 3). Gas centrifuge technology is the most prevalent, and has been used for the initial production of silicon isotopes. A number of organisations are working on other, less expensive production technologies for silicon, such as chemical exchange and laser separation. Recently, it was announced that Eagle-Picher Industries has constructed a multi-ton pilot plant in the US for the production of silicon isotopes using chemical exchange technology. Eagle-Picher already produces boron isotopes using this technology. This pilot plant will produce isotopically purified silicon tetrafluoride, which will then be chemically converted to silane and trichlorosilane by Isonics Corporation and its partners. These chemicals will then be used to produce polysilicon and epitaxial wafers using industry-standard methods.

The full range of silicon wafers can be manufactured with isotopically pure silicon (Figure 3). Bulk wafers, epitaxial wafers and SOI wafers can be manufactured via standard techniques and equipment using isotopically purified precursor materials. Epitaxial and SOI wafers can be manufactured very cost-effectively, since very little silicon-28 is required. While the benefits of these types of wafers will not be as great as with bulk silicon-28 wafers, the advantages can still be significant. Experimental work by North Carolina State University using simple power semiconductor devices (Schottky diodes) and 11-micron-thick epitaxial wafers has shown that the surface temperatures are lower on the silicon-28 epi wafers and thus the leakage currents of diodes are also lower (Figure 4). In preliminary testing with SIMOX SOI wafers, MIT's Lincoln Laboratory found significant differences in some transistor parameters, more uniform leakage data on capacitor test structures and fewer gate oxide failures with silicon-28 SOI wafers as compared with standard SOI wafers. Additional evaluation is ongoing at several research organisations and microprocessor manufacturers.

Figure 3 (below)
Silicon-28 wafer types

Figure 4 (bottom)
Effect of epi wafer type on diode leakage current (North Carolina State University data)





Since the isotope separation method is essentially a chemical process, the cost of production decreases greatly with economies of scale. As Table 2 indicates, the near-term cost of silicon-28 wafers is quite reasonable and will fall quickly as production increases. With high-volume production, the incremental material cost for isotopically pure silicon wafers should fall to about $25 for epitaxial or SOI wafers and $200–$300 for bulk prime wafers.

SUMMARY

Isotopically pure silicon has several advantages over natural silicon for high-performance devices and offers an innovative, cost-effective solution for the thermal management of next-generation microprocessors and other high-power devices. Unlike other advanced wafer technologies, there is no barrier to adoption, and industry acceptance could prove to be quite rapid. As the semiconductor industry adopts new materials for dielectrics and interconnects in the drive towards nanometre-sized transistors, atomic-scale engineering of the basic silicon substrate is the logical next step.

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